The 2012 Forum on specification & Design Languages Program

Vienna, Austria
September 18th-20th, 2012

General Chair: Jan Haase
Vienna University of Technology

FDL is an ecşi event!
# Table of Contents

Welcome ........................................................................................................................................ 4  
Keynote Speakers ............................................................................................................................ 5  
Technical Area Chairs ..................................................................................................................... 6  
Special Session Chairs .................................................................................................................... 7  
Program Committee .......................................................................................................................... 9  
Technical Area Overview ................................................................................................................. 10  
Conference Program ......................................................................................................................... 11

- **Keynote 1:** Formal Specification Level: Towards Verification-driven Design Based on Natural Language Processing ................................................................. 11
- **ABD 1:** Property-based Verification .......................................................................................... 12
- **Special Session:** Modeling & Simulation Challenges Due to Aging & Reliability of Devices ...... 12
- **EAMS 1:** Simulation & Design of Cyber-physical Systems ......................................................... 13
- **Special Session:** Invasive Programming of Heterogeneous Multi-core Systems .................... 13
- **Tutorial:** a Practical Introduction to using Event-B for Complex Hardware & Embedded System Specification & Design ..................................................................................... 14
- **ABD 2:** Languages & Tools for Probabilistic & Temporal Specifications ............................... 14
- **European SystemC Users’ Group Meeting** ............................................................................... 15
- **COMPLEX Project at FDL** ..................................................................................................... 15
- **Keynote 2:** Challenging complex system design: Model, Architecture and Standard ............. 16
- **UMES:** Effective Exploitation of the UML Profile for MARTE ............................................... 17
- **Special Session:** Smart Homes .................................................................................................. 17
- **Keynote 3:** Modeling Cyber-Physical Energy Systems .............................................................. 18
- **EAMS 2:** Verification of Mixed-Signal Systems ......................................................................... 19
- **LBSD 1:** SystemC Analysis ....................................................................................................... 19
- **Keynote 4:** Correct-by-Construction System Design: Forever a Dream or Approaching Reality ... 20
- **LBSD 2:** Architectural Aspects in Models and Languages ....................................................... 21
- **Special Session:** Energy Harvesting and Ultra-low Power Design ........................................... 21
- **LBSD 3:** System-level Behavioral Modeling and Simulation .................................................... 22
- **Special Session:** Model Based Design of Electronic Systems in Systems ............................... 22

Practical Information ......................................................................................................................... 23  
FDL Schedule .................................................................................................................................. 24
Welcome to the 15th Forum on Specification and Design Languages 2012 in Vienna.

The Forum for Design Languages (FDL) is a well established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modelling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems. Modelling and specification concepts push the development of new design and verification methodologies to system level thus providing a means for model-driven design of complex information processing systems in a variety of application domains. One of the principal advantages of FDL is that it brings together four related thematic areas and gives an opportunity to gain up-to-date knowledge in many broad areas of the fast evolving field of system design and verification.

This year, FDL has grown to offer even more the four traditional topical pillars on ABD, EAMS, LBSD, and UMES. There are special sessions on reliability, invasive programming, smart homes, energy harvesting, and model based design, and a tutorial on Event-B. Furthermore, the European SystemC Users’ Group Meeting will take place at FDL. Due to this abundance of presentations FDL now for the first time is completely two-tracked except for the four keynotes.

FDL 2012 is a conference in a very successful series. Past FDLs took place in Lausanne, Lyon, Tuebingen, Marseille, Frankfurt/Main, Lille, Darmstadt, Barcelona, Stuttgart, Sophia Antipolis, Southampton, and Oldenburg. FDL 2012 is organized by ECSI in technical cooperation with IEEE Austria Section. FDL papers will be available online via IEEEXplore after the conference and on www.ecsi.org.

Vienna University of Technology was founded in 1815 as k.k. Polytechnisches Institut (Imperial and Royal Polytechnical institute). In 1872 its name changed to Technische Hochschule (College of Technology) and then to Technische Universität Wien (Vienna University of Technology) in 1975. It is situated in the heart of Vienna. Within walking distance are the Opera House, the art nouveau Secession building, the Musikverein, home of the Vienna Philharmonic, from where the New Year’s Concert is annually broadcast around the globe, and the splendid baroque Karlskirche (Church of St. Charles). TU Vienna features its own two orchestras and Vienna’s oldest ball (TU-Ball).

General Chair:
Jan Haase
Vienna University of Technology

Jan Haase received his diploma in computer sciences at Goethe University in Frankfurt, Germany. He then became a research assistant at the technical informatics department at Frankfurt University. There he focused on the field of computer architectures, dynamic and distributed parallel computation, middlewares, and embedded systems, resulting in his PhD thesis about the scalable, dataflow-driven virtual machine (SDVM). Since 2007, he is senior researcher and project leader at the Vienna University of Technology. His research interests include hardware/software co-design, design methodologies for heterogeneous (AMS+HW/SW) systems, power consumption optimization and automatic parallelization. He is IEEE senior member and past IEEE Austria Section Chair. He is author and co-author of more than 70 publications. He is associate editor of IEEE Transactions on Industrial Informatics and served and serves as program (co-) chair or member in several program committees of international conferences like IECON, AFRICON, DATE, FDL, CSNDSP, ICIEA, Austrochip, and smaller workshops.
Rolf Drechsler received the Diploma and Dr. Phil. Nat. degrees in computer science from J.W. Goethe University Frankfurt am Main, Frankfurt am Main, Germany, in 1992 and 1995, respectively. He was with the Institute of Computer Science, Albert-Ludwigs University, Freiburg im Breisgau, Germany, from 1995 to 2000, and with the Corporate Technology Department, Siemens AG, Munich, Germany, from 2000 to 2001. Since October 2001, he has been with the University of Bremen, Bremen, Germany, where he is currently a Full Professor and the Head of the Group for Computer Architecture, Institute of Computer Science. Since 2011 he is also the Director of the Cyber-Physical Systems group at the German Research Center for Artificial Intelligence (DFKI) in Bremen. His current research interests include the development and design of data structures and algorithms with a focus on circuit and system design.

Sébastien Gérard is leading the LISE laboratory, Laboratory of Model Driven Engineering for Embedded Systems, at CEA LIST, the . His research interests include correct-by-construction specification and design of complex systems, model-based engineering of RT/E systems and modeling language engineering. He is the CEA representative at OMG for more than 10 years. In particular, he is the chair of the MARTE standardization task force. He is also leading the open-source project, Papyrus (www.eclipse.org/papyrus), the UML modeling tools of Eclipse. In 1995, he has a diploma in mechanics and aeronautics from the ENSMA high-school, and in 2000 he obtained a PhD diploma in Computer Science.

Peter Palensky is Principal Scientist at the AIT Austrian Institute of Technology / Energy Department. Before that he was Head of Business Unit "Sustainable Building Technologies" at the AIT, CTO of Envidatec Corp., Hamburg, Germany, associate Professor at the University of Pretoria, South Africa, Department of Electrical, Electronic and Computer Engineering, University Assistant at the Vienna University of Technology, Austria, and researcher at the Lawrence Berkeley National Laboratory, California. He is active in international committees like ISO, IEEE and CEN. His main research fields are complex energy systems and intelligent buildings.

Ingo Sander received the MSc degree in Electrical Engineering from the Technical University of Braunschweig, Germany, in 1990 and the PhD degree from KTH - Royal Institute of Technology, Sweden, in 2003. Between 1991 and 1993 he has worked as system design engineer at Ericsson, Sweden. In 1993 he joined KTH, where he since 2005 holds a position as associate professor in Electronic System Design. His main research interests are located in the area of design methodologies for embedded systems. His current research is aiming towards predictable performance of real-time applications on multi-processor platforms by integration of formal models into the design flow.
EAMS TA Chair: Prof. Christoph Grimm, TU Kaiserslautern

Christoph Grimm received his Diploma in Electrical Engineering in 1994 from TU Darmstadt and his Ph.D. in Computer Science in 1999 from University of Frankfurt. He worked as post-doc at Universities of Frankfurt and Hannover. Since 2006 he is full professor for Embedded Systems at TU Vienna’s Institute of Computer Technology. Christoph Grimm’s research interest is design methodology of analog/mixed-signal systems and design of SoC for power management in future green homes. He contributed the development of IEEE 1076.1 (VHDL-AMS) and IEEE 1076.6 (VHDL-SWG). In 2001, was co-founder of the OSCI SystemC AMS study group. He serves the OSCI AMS WG as vice chair and contributed as co-author to the SystemC AMS 1.0 extensions standard and the SystemC AMS users’ guide. Christoph Grimm has contributed to the major conferences as PC or SC member or chair. He is head of the scientific advisory board of OVE and of the Austrian Society for Microelectronic Systems, speaker of the research cluster "AutCom" of TU Vienna, and scientific advisor for microelectronic and automotive companies. He is member of IEEE, OVE, and VDE.

ABD TA Chair: Prof. Dominique Borrione, TIMA

Dominique Borrione has been a Professor at the University of Grenoble since 1988. Since January 2007, she is the director of TIMA Laboratory. From the University of Grenoble, she received the MSc in Computer Science in 1972, the PhD in Computer Science in 1976, and the Thèse d’Etat in 1981. Before joining TIMA, she was director of the ARTEMIS Laboratory from 1991 to 1995. She was a team leader at ARTEMIS (1988-1995), then at TIMA (1996-2006). From Dec. 1983 to August 1988, she was a Professor at the University of Marseille. She developed the theme of formal methods methods in hardware design, particularly taking as as input designs described in VHDL. Most of her research has been supported by contracts, through industrial and academic cooperative projects in the context of the ESPRIT and MEDEA European programs. Professor Borrione has published over 90 refereed journal papers, international refereed conference papers, and book chapters. She has been a member of numerous working groups, and program committees of international conference and workshop series (CHDL, CHARME/FMCAD, DATE, SBCCI, VLSI-SOC). She was program chair of CHDL’81, DATE’99, CHARME’05, and FDL’09.

LBSD TA Chair: Martin Radetzki, University of Stuttgart

Martin Radetzki received the Dipl.-Inform. and Dr.-Ing. degrees in Computer Science from Oldenburg University in 1996 and 2000, respectively. From 2000 until 2005, he held industry positions as a design engineer and as a design methodology project manager. Since 2005, he has been a professor of Embedded Systems Engineering in the faculty of Computer Science and Electrical Engineering, University of Stuttgart, Germany. His research group contributes to the Cluster of Excellence on Simulation Technology, SimTech. His main research interests are in the fields of specification and design of embedded systems functionality and architecture and the corresponding aspects of system simulation and reliability.

UMES TA Chair: Julio Medina, University of Cantabria

Julio Medina is graduated as Electronics Engineer from the Universidad Nacional de Ingeniería, Perú, in 1987. He obtained the Master in Real-Time Systems (1993) and the Doctorate in Telecommunications Engineering (2005) from the Universidad de Cantabria, Spain. He developed electronics and embedded software for nuclear instrumentation in the Peruvian Nuclear Research Center, then worked as assistant professor in electronics instrumentation and software engineering, and did research on distributed real-time systems. During the doctorate period he concentrated on the modeling of real-time systems developed with object-oriented techniques, being later co-author of the UML Profile for MARTE of the OMG in a post-doctorate research at the Commissariat a l’Energie Atomique in France. Currently he is lecturer in the Universidad de Cantabria and does research in several European projects. His main research topics include the modeling of real-time distributed systems for schedulability analysis, the UML representation of such models, and its usage for modular and component-based development strategies.
Tom J Kazmierski, University of Southampton

**Special Session Chair: Energy Harvesting and Ultra-Low Power Design**

Tom Kazmierski received the M.S. degree in Electronic Engineering from the Warsaw University of Technology, Warsaw, Poland, in 1973 and the Ph.D. degree from the Military University of Technology, Warsaw, in 1976. Currently he is a Senior Lecturer in the School of Electronics and Computer Science, University of Southampton, Southampton, U.K., where he pursues research into numerical modelling, simulation, and synthesis techniques for computer-aided design of very large scale integration (VLSI) circuits and mixed-technology systems. From 1989 to 1990 he was a Lecturer in Microelectronics at the Griffith University in Brisbane, Australia. From 1990 to 1991 Tom worked as a Visiting Research Scientist at the IBM VLSI Technology Division, San Jose, CA, USA where he developed and patented synchronisation techniques for multi-solver simulation backplanes. He has contributed to the development of the VHDL-AMS standard by the IEEE, served as Chair of the IEEE DASC P1076.1 (VHDL-AMS) Working Group from 1999 to 2005. He has published over 100 papers and given a number of invited talks and tutorials mostly in the area of analogue and mixed signal synthesis and hardware description languages. In recent years he has been working on web-based electronic design frameworks and applications of VHDL-AMS to high-level system modelling and synthesis, including automated analogue and mixed-signal synthesis for ASIC design, synthesis of artificial VLSI neural networks and performance modelling of mixed-technology electromechanical systems.

Christian Haubelt, University of Rostock

**Special Session Chair: Invasive Programming of Heterogeneous Multi-Core Systems**

Christian Haubelt is a Professor of Embedded Systems at the University of Rostock, Germany. He received his diploma degree in Electrical Engineering from the University of Paderborn, Germany, in 2001. He finished his Ph.D. in Computer Science and his Habilitation (postdoctoral lecture qualification) in Computer Engineering at the University of Erlangen-Nuremberg, Germany, in 2005 and 2010, respectively. From 2010 to 2011 he has been a Substitute Professor of Computer Engineering at the University of Potsdam, Germany. His research interests include design automation for embedded computing systems, programming of heterogeneous Multi-Processor Systems-on-Chip (MPSoC), and design space exploration.

Domenik Helms, University of Oldenburg

**Special Session Chair: Modeling and Simulation Challenges Due to Aging and Reliability of Devices**

Domenik Helms is the Manager of the technology cluster ‘Design of HW/SW systems’ at OFFIS research institute, Germany. He received his Diploma degree in theoretical physics for a numerical analysis of the quantum hall effect in 2001 and finished his Ph.D. (Dr. rer. nat.) in 2009 on leakage models for high level power estimation from the University of Oldenburg. His research interests are analysis, description and modelling of physical effects in recent transistor geometries, such as leakage currents, process variation, ageing and failure mechanisms, and reliability and robustness of embedded systems.
Sumit Adhikari, Vienna University of Technology

Special Session Co-Chair: Model Based Design of Electronic Systems in Systems

Sumit Adhikari completed Master of Technology from Indian Institute of Technology, Kharagpur. He worked for several years with industry, for Qual Core Logic Inc. and austriamicrosystems AG. He joined ICT, TU Vienna on April 2010 as a scientist. His interest lies on RF transceivers, analogue signal processing, digital signal processing, mixed signal signal path designing, analogue signal path designing and modelling, sensor dynamics and sensor modelling, development of analogue-mixed signal HDL, high level solvers for analogue-mixed signal domain. His domain expertise lies on Automotive sensor actuator systems, RF-Wireless systems, Industrial electronic systems and Instrumentation applications.

Slobodanka Tomic, FTW

Special Session Chair: Smart Homes

Dr. Slobodanka Tomic received her Ph.D. degree in Electrical and Computer Engineering from the Vienna University of Technology (TU Wien), Austria. Since 2005 Mrs. Tomic works as a Senior Researcher and Project Manager at The Telecommunications Research Centre Vienna (FTW), in national and EU projects in the area of “Networked Services”. Prior to that, Mrs. Tomic was working with the industry and as a researcher at the TU Wien. From 2009 - 2010 Mrs. Tomic was involved in the nationally funded project “Semantic Smart Metering (SESAME)”. Since March 2010 she is managing the national project “Grid Responsive Energy Efficient Networked Home (GREEN HOME)”. Her current research includes energy economics, computational economics, modeling optimization and simulation of energy markets, agent-based systems for future market participation of grid responsive home environments in the Smart Grid, semantic enablers and computational intelligence for the user-centric control of energy aware smart homes, and service and communication enablers for data economies.
Technical Area Overview

Conference Scope

FDL is an international forum to exchange experiences and promote new trends in the application of languages, their associated design methods and tools for the design of electronic systems. The Forum is organized around four Thematic Areas (TA) described below and this year includes five special sessions and a tutorial on Event-B. The European SystemC Users’ Group Meeting meeting is also held in conjunction with the Forum.

**ABD TA: Assertion Based Design, Verification & Debug**

**TA Chair:** Dominique Borrione, TIMA

The ABD Thematic Area welcomes research contributions, tool demonstrations, reports on standardization activities and effective applications in all aspects of innovative property expression and processing, with an emphasis on frontier design levels, verification, automatic synthesis and mechanized debug aids. The assertion of formal properties provides a uniform expression of expected system behaviour, or constraints that are assumed on the environment, for a variety of design tasks: verification of functional correctness, generation of test stimuli, synthesis of observation monitors and on-line tests, model checking on the reachable state space, direct synthesis from assertions, etc. Standardized formalisms such as PSL and SystemVerilog assertions were initially intended for synthesizable RTL; their application is now considered at transaction levels and for mixed system designs.

**LBSD TA: Language-Based System Design**

**TA Chair:** Martin Radetzki, University of Stuttgart

The LBSD TA addresses language-based modelling and design techniques for simulation, debugging, transformation, and analysis of digital hardware/software embedded systems. Contributions are welcome on innovative applications, language or library design, and methodological aspects. SystemC has undergone restandardization to keep up to date with users' needs. Hence, contributions on new applications and evolution of SystemC are highly welcome. Equally welcome are papers dealing with SystemVerilog, functional languages, UML in conjunction with executable specification, and emerging languages. Aspects of methodology, interoperability, simulation semantics, and models of computations will find an audience just like embedded software modelling techniques and technology or domain specific approaches, e.g. for signal processing applications or reconfigurable computing platforms. Moreover, transaction level modelling (TLM) with any language, IP-based system design (e.g. IP-XACT), modelling aspects in system synthesis, innovative industrial case studies, and efficient parallel simulation of high-level models are in scope.

**EAMS TA: Embedded Analog and Mixed-Signal System Design**

**TA Chair:** Christoph Grimm, TU Kaiserslautern

The EAMS TA addresses design, modeling, and verification of heterogeneous systems that include significant part of "analog" or "continuous" behavior such as cyber physical systems, wireless sensor networks, and of course analog/mixed-signal circuits. A new challenge is the tight interaction of analog or physical components with - maybe distributed - digital hardware/software systems. Topics of interest include specification, modeling, simulation, (symbolic) analysis, verification, design, (virtual) prototyping, and synthesis of analogue, mixed-signal, and mixed-technology systems, wireless sensor nets, and cyber physical systems. Focus of contributions should be on languages, models, representations, and tools such as VHDLM-AMS, SystemC-AMS, Modelica, Matlab/Simulink, etc. The EAMS TA aims at presenting research activities, design experiences, and standardization issues related to these topics.

**UMES TA: UML and MDE for Embedded System Specification & Design**

**TA Chair:** Julio Medina, University of Cantabria

Model driven methods, mostly based on the Unified Modelling Language, increasingly support semi-formal methods for system level design of complex embedded systems including multi-core, highly programmable platforms and heterogeneous Systems-on-Chip. UMES related research topics in this field are Executable UML, model driven development, model transformations, UML semantics, meta-modelling, e.g., for SystemC and other System Description Languages or HDLs, UML profiles, e.g. SysML, MARTE, UML for SoC, and formalization of UML towards domain specific languages for simulation and synthesis. Other welcomed topics are standardization work, modelling languages for real-time and embedded systems, model driven techniques for performance analysis, validation and verification, SDL, AADL, OCL, XMI, and practical design experiences with UML or in general model driven engineering (MDE) approaches.
The steadily increasing complexity of the design of embedded systems led to the development of both an elaborated design flow that includes various abstraction levels and corresponding methods for synthesis and verification. However, until today the initial system specification is provided in natural language which is manually translated into a formal implementation e.g. at the Electronic System Level (ESL) by means of SystemC in a time-consuming and error-prone process. We envision a design flow which incorporates a Formal Specification Level (FSL) thereby bridging the gap between the informal textbook specification and the formal ESL implementation. Modeling languages such as UML or SysML are envisaged for this purpose. Recent accomplishments towards this envisioned design flow, namely the automatic derivation of formal models from natural language descriptions, verification of formal models in the absence of an implementation, and code generation techniques, are briefly reviewed.
The first paper is about the static analysis of constraints that define the environment of an IP, typically a communication protocol, and guarantee that the environment is not over-constrained. The second paper presents the use of affine arithmetic to model typical properties of mixed-signal devices and check the impact of parameter deviations on the system behavior. The third contribution discusses the use of verified CTL properties about a system components to generate efficient component abstractions and verify a global property on their composition.

**Formal Plausibility Checks for Environment Constraints**
Binghao Bao, Markus Wedler, Dominik Stoffel and Wolfgang Kunz (University of Kaiserslautern)

**Assertion Based Verification of Signal Processing Systems with Affine Arithmetic**
Carna Radojicic, Florian Schupfer, Michael Rathmair and Christoph Grimm (Institute of Computer Technology TU Wien)

**An Efficient Refinement Strategy Exploiting Component Properties in a Cegar Process**
Syed Hussein Syed Alwi, Cécile Braunstein and Emmanuelle Encrenaz (LIP6 - CNRS UMR 7606)

This session gives insight into ageing phenomena occurring in recent and approaching nanometric technology generations. After a survey of all relevant mechanisms, modelling and simulation methodologies from single transistor description towards system level modelling are presented. It will be discussed, how the device view, describing parametric drifts for individual circuits can be translated into a top-down view of failure probabilities. Current status of solutions and open questions for the EDA community shall be worked out.

**Aging in CMOS Devices: From Microscopic Physics to Compact Models**
Tibor Grasser (Vienna University of Technology)

**Compact Model Coding: A Case-Study Using the Verilog-AMS Language**
Laurent Lemaitre (Noovela Consulting)

**Lifetime Simulation Methods for Integrated Circuit Simulation**
A. Steinmair, H. Gensinger and Ehrenfried Seebacher (Austriamicrosystems AG)

**A Map Based System Level Aging Model**
Reef Eilers, Malte Metzdorf (OFFIS) and Wolfgang Nebel (University of Oldenburg)

**Lunch**
12:30-14:00
In Cyber-Physical Systems, physical parts with a continuous time model, and software or even information systems with logic time are strongly interwoven. This leads to new challenges for design and modeling/simulation. The first paper in this session describes the benefits of considering properties of an application during the design process. The second and the third paper describe frameworks for modeling and simulation. The second is focused on modeling the networking aspect; the third one deals with implementation of the computing systems.

**QoC-Oriented Efficient Schedule Synthesis for Mixed-Criticality Cyber-Physical Systems**
Reinhard Schneider, Dip Goswami, Alejandro Masrur and Samarjit Chakraborty
(Technical University of Munich)

**Unified and Comprehensive Electronic System Level, Network and Physics Simulation for Wirelessly Networked Cyber Physical Systems**
Javier Moreno, Markus Damm, Jan Haase (Vienna University of Technology), Christoph Grimm (TU Kaiserslautern), and Edgar Holleis (Tridonic)

A **Unified Platform for Design and Verification of Mixed-Signal Systems Based on SystemC AMS**
Yao Li, Ramy Iskander, Farakh Javid and Marie-Minerve Louerat (UMPC LIP6)

**SS: Invasive Programming of Heterogeneous Multi-core Systems**
Chair: Christian Haubelt, University of Rostock
Room: EI10

The idea and novelty of invasive computing is to introduce resource-aware programming support in the sense that a given program gets the ability to explore and dynamically spread its computations to neighbour processors similar to a phase of invasion, then to execute portions of code of high parallelism degree in parallel based on the available (invasive) region on a given multi-processor architecture. Afterwards, once the program terminates or if the degree of parallelism should be lower again, the program may enter a retreat phase, deallocate resources and resume execution again, for example, sequentially on a single processor. In order to support this idea of self-adaptive and resource-aware programming, not only new programming concepts, languages, compilers and operating systems are necessary but also revolutionary architectural changes in the design of MPSoCs (Multi-Processor Systems-on-a-Chip) must be provided so to efficiently support invasion, infection and retreat operations involving concepts for dynamic processor, interconnect and memory reconfiguration. This special session covers the concept of invasive computing, necessary architectural changes, and resource-aware programming of MPSoCs.

**An Integrated Simulation Framework for Invasive Computing**
Michael Gerndt, Andreas Herkersdorf, Andreas Hollmann, Marcel Meyer, Josef Weidendorfer, Thomas Wild and Aurang Zabi (Technische Universität München), Frank Hannig and Sascha Roloff (University of Erlangen-Nuremberg)

**Invasive Computing - Concepts and Overheads**
Jürgen Teich, Andreas Weichsrgartner, Benjamin Oechslein and Wolfgang Schröder-Preikschat
(University of Erlangen-Nuremberg)

**Invasive Computing with iOMP**
Michael Gerndt, Andreas Hollmann, Marcel Meyer, Martin Schreiber and Josef Weidendorfer
(TEchnische Universität München)
Event-B is a proof-based modelling language and method that enables the systematic development of specifications using a formal notion of refinement. The Rodin platform is the Eclipse-based IDE that provides automated support for Event-B modelling, refinement and mathematical proof. This tutorial will show how an abstract, untimed specification can be represented in Event-B and then systematically refined to a timed, architectural representation from which a software or hardware description can be derived for each architectural component. We will show how, at each refinement stage, the proofs needed to verify that the concrete model meets its abstract specification are generated automatically by Rodin. Having proved that the refinement is correct, the Rodin animator and model checker, ProB, is then used to execute the model, verify invariants and temporal properties and show absence of deadlock. We will also show how PSL or SystemVerilog assertions can be derived from the invariants and temporal properties developed in Rodin for use in a traditional, simulation-based verification flow.

Coffee Break
15:30-16:00

The first paper defines a variation of bounded LTL, and its trace semantics, for the specification of reliability requirements for embedded systems; action traces are processed to compute the reliability satisfaction for a given action schedule. The second (invited) paper is an introduction to the MODEST specification language and its toolset.

Reliability Annotations to Formal Specifications of Context Sensitive Properties in Embedded Systems
Aritra Hazra, Priyankar Ghosh and Pallab Dasgupta (Indian Institute of Technology Kharagpur)

MODEST – A Unified Language for Quantitative Models (Invited presentation)
Arnd Hartmanns (Saarland University)

FDL Planning Committee Meeting
Room: CDO404 (2nd floor)
This meeting is organized as panel discussion focused on the technical and industrial challenges for SystemC.

Opening
Frank Oppenheimer, OFFIS Research, DE

Accellera SystemC Initiative Update
Dennis Brophy, Mentor Graphics & ASI, US

Panel Discussion: Technical Challenges for Industrial SystemC Application
Moderation: Frank Oppenheimer, OFFIS Research, DE
Panelists:
Albrecht Mayer, Infineon Technologies, DE
Dennis Brophy, Mentor Graphics & ASI, US
Martin Radetzki, University of Stuttgart, DE
Jack Donovan, Duolog Technologies, IE

Closing
Frank Oppenheimer, OFFIS Research, DE

Reception & Refreshments

The European SystemC Users Group Meeting is supported by ECSI, the Open SystemC Initiative, and these Global Sponsors:
Accellera, ARM, Cadence, Circuit Sutra, Forte, Synopsys, Mentor Graphics, Synopsys
www.systemc.org

The COMPLEX (COdesign and power Management in PLatform-based design space EXploration) consortium develops a new design environment for platform-based design-space exploration offering developers of next-generation mobile embedded systems a highly efficient design methodology and tool chain. The integrated environment allows iterative exploration and refinement of advanced applications to meet market requirements. The design technology in particular enables fast simulation and explores the use of different implementations at Electronic System Level (ESL) with up to bus-cycle accuracy at the earliest instant in the design cycle. The main objectives are:

- Highly efficient and productive design methodology and holistic framework for design space exploration of embedded HW/SW systems.
- Combination and augmentation of well-established ESL synthesis & analysis tools into a seamless design flow enabling performance & power aware virtual prototyping of the HW/SW system.
- Interfacing next-generation model-driven SW design approach and industry standard model-based design environments.
- Multi-objective co-exploration for assessing design quality and optimizing the system platform with respect to performance, power, and reliability metrics.
- Fast simulation and assessment of the platform at ESL with up to bus-cycle accuracy at the earliest instant in the design cycle.
- Optimization benefits from run-time mode adaptation techniques, such as dynamic power management or application adaptation to varying workloads.

COMPLEX related paper presented at FDL 2012:
A Model-Driven Methodology for the Development of SystemC Executable Environments
Fernando Herrera, Pablo Peñil, Héctor Posadas and Eugenio Villar (University of Cantabria)

More information about the COMPLEX project can be found at http://complex.offis.de
Development of increasingly more sophisticated dependable real-time and embedded systems requires new paradigms, since contemporary code-centric approaches are reaching their limits. Experience has shown that model-based engineering using domain-specific modeling languages is an approach that can overcome many of these limitations. Moreover, managing complexity of system development requires designing sound and efficient architectures using as much as possible standard-based solution to reduce the cost of developments. This keynote will talk about aforementioned paradigms, model and architecture, and put these latter in perspective of standardization.
UMES: Effective Exploitation of the UML Profile for MARTE
Chair: Julio Medina, University of Cantabria
Co-chair: Gjalt De Jong, ArchWorks
Room: EI9

This session presents two applications of the UML/MARTE standard. The first proposes a methodology to model a systems external stimuli environment, and an approach to generate a testbench in executable SystemC. The second discusses how to model and simulate jamming attacks in Wireless Sensor Networks. The final open discussion panel in this session aims at seeking for further prospective exploitation of the MARTE profile and other related standardization efforts at the OMG.

A Model-Driven Methodology for the Development of SystemC Executable Environments
Fernando Herrera, Pablo Peñil, Héctor Posadas and Eugenio Villar (University of Cantabria)

Modeling and Simulation of Secure Wireless Sensor Network
Alvaro Diaz Suarez, Pablo Peñil and Pablo Sanchez (University of Cantabria),
Juan Sancho and Juan Rico (TST)

Open Discussion Panel: MARTE Exploitation Perspectives
Current Standardization Trends: Foundational UML and A Precise Semantics for UML Composite Structures

SS: Smart Homes
Chair: Slobodanka Tomic, FTW
Co-Chair: Jan Haase, Vienna University of Technology
Room: EI10

Next Generation Smart Homes will offer a broad range of innovative services to their residents by using a variety of intelligent connected devices, including Home Gateway with the broadband Internet access, intelligent appliances, sensors and actuators, cameras, smart meters for electricity, gas, water, remote heating, entertaining devices, home energy production equipment, smart displays, mobile phones, etc. By combining home networking with Internet access Smart Homes can serve their customers no matter where they are and support them in making decisions about home control. The market for connected devices and service is huge and rapidly growing and is of strategic priority for many sectors, such as mobile industry, energy, entertainment, home security, assisted living, and health. The Smart Home service platform needs to host applications of different providers and enables innovative device, service and customer management interactions, and as a result not only the opportunities and benefits, but also the challenges of Smart Connected Home design increase as the heterogeneity of services and devices raises. Although the vision of the Smart Homes is well established; there is still a number of open issues which require attention in order for the vision to realize. This SS aims at bringing together researchers working in the area of Smart Homes to discuss their experiences and achievements and identify the most interesting trends in the Smart Home Evolution.

Green Home - a Concept and a Study of Grid Responsiveness
Slobodanka Tomic (FTW) and Jan Haase (Vienna University of Technology)

A PLC Broadband Channel Simulator for Indoor Communications
Giuseppe Marrocco, Driton Statovci (FTW Forschungszentrum Telekommunikation Wien GmbH),
and Steffen Trautmann (Lantiq A GmbH)

Android Based Home Appliances Simulator
Michael Rathmair and Jan Haase (Vienna University of Technology)

Using Circuit Simulation Techniques for Building Automation Simulations
Joseph Wenninger and Jan Haase (Vienna University of Technology)
The energy system faces a number of substantial changes. Distributed energy resources are on the rise, smart grids combine information technology, stochastic renewable energy sources feed into the mid- and low-voltage grid and electric mobility will make things not easier either. In addition, this future energy system is expected to allow for new market models, active customer (to be called “prosumer”) participation and links to other systems. The expected complexity exceeds the scope of established modeling and simulation tools. This talk will be about the first steps towards hybrid modeling and co-simulation of complex energy systems.

**FDL registration includes free access to S4D sessions!**
EAMS 2: Verification of Mixed-Signal Systems
Chair: Torsten Maehne, UPMC
Co-Chair: Sumit Adhikari, Vienna University of Technology
Room: El9

This session includes contribution that advance state of the art in verification of mixed-signal systems. The first paper gives a method to emulate analog loads for in-lab experiments. The second paper describes a method for more efficient simulation of linear systems in SystemC AMS. The third paper proposes a method for specifying assertions for analog circuits.

Configurable Load Emulation using FPGA and Power Amplifiers for Automotive Power ICs
Manuel Harrant, Thomas Nirmaier, Fabrizio Dona, Georg Pelz (Infineon Technologies), and Christoph Grimm (TU Kaiserslautern)

A SystemC AMS extension for controlled modules and dynamic step sizes
Christiane Reuther and Karsten Einwich (Fraunhofer IIS/EAS Dresden)

Analog Assertion-Based Verification on Partial State Space Representations using ASL
Sebastian Steinhorst (TUM CREATE Centre for Electromobility Singapore) and Lars Hedrich (Goethe-Universitaet Frankfurt am Main)

LBSD 1: SystemC Analysis
Chair: Peter Flake, Elda Technologies
Co-Chair: Frank Oppenheimer, OFFIS
Room: El10

Static and dynamic analysis are essential techniques for extracting information about a design being modeled or the model itself. This session deals with analysis of SystemC models. The papers address high-level power estimation, detection of nondeterminism anomalies, and localization of features in complex models.

TLM POWER3: Power Estimation Methodology for SystemC TLM 2.0
David Greaves (University of Cambridge) and Muhammad Mehboob Yasin (King Faisal University, Al-Ahase)

Scandal: SystemC Analysis for NonDeterminism AnomaLies
Christoph Schumacher, Jan Henrik Weinstock, Rainer Leupers and Gerd Ascheid (RWTH Aachen University, ICE)

Localizing Features of ESL Models for Design Understanding
Marc Michael, Daniel Grosse and Rolf Drechsler (University of Bremen)
Advances in process technology have led to extremely powerful many-core platforms, but in practice it is very difficult to exploit their inherent potential. Instead, in particular in the real-time domain, the verification costs often dominate the design costs due to a lack of design methodologies capable of handling the increasing complexity of large heterogeneous and inherently parallel embedded systems. Simulation is still the dominating verification technique in industry and can only indicate, but not prove the correctness of an implementation. In recent years, research has significantly improved the possibility for a correct-by-construction design flow, especially in areas like predictable architectures and models of computation. The keynote discusses the current situation, analyzes prerequisites and provides suggestions towards a correct-by-construction design flow, which could drastically reduce the verification costs.
Each abstraction level in the design process has an architectural view that takes into account the specifics of the implementation building blocks at that level. This session is devoted to such architectural aspects. It deals with the programming of homogeneous manycore systems, the modeling of heterogeneous virtual system platforms, and the language-based design of reversible logic.

**Minimal MPI as Programming Interface for Multicore System-on-Chips**
Adan Kohler, Juan Manuel Castillo-Sanchez, Joachim Groß and Martin Radetzki (University of Stuttgart)

**A Functional Language for Describing Reversible Logic**
Michael Kirkedal Thomsen (University of Copenhagen)

**Integrating Virtual Platforms into a Heterogeneous MoC-Based Modeling Framework**
Gilmar Silva Beserra (University of Brasilia), Seyed Hosein Attarzadeh Niaki and Ingo Sander (KTH - Royal Institute of Technology)

**SS: Energy Harvesting and Ultra-low Power Design**
Chair: Tom Kazmierski, University of Southampton
Room: EI10

**Energy Harvesting for self-sufficient wireless sensor nodes in Body Area Networks** (Invited presentation)
Thomas Herndl (Infineon Austria)

**Example-Driven Interconnect Synthesis for Heterogeneous Coarse-Grain Reconfigurable Logic**
Clifford Wolf, Johann Glaser, Florian Schupfer, Jan Haase (Vienna University of Technology), and Christoph Grimm (TU Kaiserslautern)

**Minimum Energy Point of Sub-threshold Operated Pass-transistor Circuits**
Aleksandar Pajkanovic (University of Banja Luka), Tom Kazmierski (University of Southampton), and Branko Dokic (University of Banja Luka)
Behavioral models abstract away implementation details to achieve goals such as capturing the design intention or achieving fast simulation. The papers in this session deal with several aspects of behavioral models. They cover efficient integration of RTL models into high-level simulation, heterogeneous modeling in a functional programming framework, and uncertainty representation in system level models.

**Transformation of Event-Driven HDL Blocks for Native Integration into Time-Driven System Models**  
Ralph Görgen (OFFIS), Jan-Hendrik Oetjens (Robert Bosch GmbH), and Wolfgang Nebel (Carl von Ossietzky University Oldenburg)

**Formal Heterogeneous System Modeling with SystemC**  
Seyed Hosein Attarzadeh Niaki and Ingo Sander (KTH Royal Institute of Technology), Mikkel Koefoed Jakobsen (Technical University of Denmark), and Tero Sulonen (DA-Design Oy)

**Extended Framework for System Simulation with Affine Arithmetic**  
Michael Rathmair, Florian Schupfer, Carna Radojicic (Vienna University of Technology) and Christoph Grimm (TU Kaiserslautern)

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Model based design of system architectures and optimization of those architectures at highest level of abstraction is gaining importance in modern day system level applications and designs. However, these complex systems need to be resolved and dened accurately at system level which is done by modelling of complete system. The process of efficient modelling and use of those models to optimize the system is often misunderstood by both academia and industry. This special session is intended to give a good overview on current works in this area and problems and solutions in specific industry use cases.

**Polynomial-Metamodeling Assisted Fast Power Optimization of Nano-CMOS PLL Components**  
Oleg Garitselov, Saraju Mohanty and Elias Kougianos (University of North Texas)

**Model-Based Progressive Design and Verification of an Integrated CMOS Magnetic Sensor for Automotive Applications**  
Gael Close (Melexis) and Gjalt de Jong (Melexis, ArchWorks)

**Fast Optimization of Analog Amplifier Architecture Using Simulated Annealing**  
Sumit Adhikari, Florian Schupfer (Vienna University of Technology), and Christoph Grimm (TU Kaiserslautern)

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**Closing**  
15:30  
Room: EI9
Welcome to Vienna

Welcome to Vienna, the largest and most populous city in Austria as well as a cultural, economic, and political centre.

The 15th annual FDL Conference is held at the Vienna University of Technology, situated in the heart of Vienna. Within walking distance are the Opera House, the art nouveau Secession building, the Musikverein, home of the Vienna Philharmonic, from where the New Year’s Concert is annually broadcast around the globe, and the splendid baroque Karlskirche (Church of St. Charles).

Vienna University of Technology
Gusshausstr. 27-29, 1040 Wien
Building C, part CA
(main entrance of C)

Language
The language of the conference will be in English.

Rooms
FDL: EI9 & EI10
Event B Tutorial: CDO404
FDL PC Meeting: CDO404
ESCUG Meeting: EI10

Conference/Registration Hours:
- Tuesday 8:30 – 17:30
- Wednesday 8:30 – 16:30
- Thursday 9:00 – 15:30

Social Event
The 2012 FDL Social Event will start with an exclusive tram ride around the Ringstrasse, a circular road surrounding the Innere Stadt district of Vienna, Austria and one of its main sights. Following the historic tram ride, the participants will be led through a guided tour at the Albertina, one of the most famous museums in the world. The Social Event will then conclude with dinner at the Augustinerkeller restaurant near the Albertina.

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