The 2011 Forum on specification & Design Languages Program

Oldenburg, Germany
September 13th-15th, 2011

General Chair:
Frank Oppenheimer
OFFIS, Germany

FDL is an ecsi event!
# Table of Contents

Welcome .......................................................................................................................... 4  
Keynote Speakers ........................................................................................................... 5  
Technical Area Chairs .................................................................................................. 6  
Program Committee ...................................................................................................... 7  
Technical Area Overview ............................................................................................... 8  
Conference Program ..................................................................................................... 9  

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDL Welcome, Keynote 1</td>
<td>9</td>
</tr>
<tr>
<td>EAMS 1: Design and Optimisation of Heterogeneous Systems</td>
<td>10</td>
</tr>
<tr>
<td>Tutorial 1</td>
<td>10</td>
</tr>
<tr>
<td>EAMS 2: Circuit Modelling and Design</td>
<td>11</td>
</tr>
<tr>
<td>Tutorial 2</td>
<td>11</td>
</tr>
<tr>
<td>ABD panel</td>
<td>12</td>
</tr>
<tr>
<td>European SystemC Users’ Group Meeting</td>
<td>13</td>
</tr>
<tr>
<td>Keynote 2</td>
<td>14</td>
</tr>
<tr>
<td>ABD 1: Assertion-Based Technology for Verification and Synthesis</td>
<td>15</td>
</tr>
<tr>
<td>LBSD 1: Syntactic Sugar? - Language Design and Semantics</td>
<td>15</td>
</tr>
<tr>
<td>UMES 1: UML Based Validation, Verification, and Testing</td>
<td>16</td>
</tr>
<tr>
<td>Tutorial: Parallelize your TLM Simulation of MPSoC on SMP Workstations!</td>
<td>16</td>
</tr>
<tr>
<td>UMES 2: MARTE at Work &amp; Standardization Trends</td>
<td>17</td>
</tr>
<tr>
<td>LBSD 2: Hurry up! - Speedy Simulation Techniques</td>
<td>17</td>
</tr>
<tr>
<td>Keynote 3</td>
<td>18</td>
</tr>
<tr>
<td>LBSD 3: In the End, Implement! - Design Refinement and Implementation</td>
<td>19</td>
</tr>
<tr>
<td>LBSD 4: Evaluate This! - System-Level Modelling and Evaluation</td>
<td>20</td>
</tr>
<tr>
<td>Complex Project at FDL 2011</td>
<td>21</td>
</tr>
<tr>
<td>FDL Books</td>
<td>22</td>
</tr>
<tr>
<td>Practical Information</td>
<td>23</td>
</tr>
<tr>
<td>FDL Schedule</td>
<td>24</td>
</tr>
</tbody>
</table>
The Forum for Design Languages (FDL) is a well established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design and verification languages to the design, modelling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems. Modelling and specification concepts push the development of new design and verification methodologies to system level thus providing a means for model-driven design of complex information processing systems in a variety of application domains. One of the principal advantages of FDL is that it brings together four related thematic areas and gives an opportunity to gain up-to-date knowledge in many broad areas of the fast evolving field of system design and verification.

FDL 2011 held in Oldenburg, Germany, from 13 to 15 September 2011 is the fourteenth FDL conference following a series of highly successful events that took place in Lausanne, Lyon, Tübingen, Marseille, Frankfurt am Main, Lille, Darmstadt, Barcelona, Stuttgart, Sophia Antipolis, and Southampton. FDL is organized in technical cooperation with the IEEE. FDL papers will be available online via IEEEXplore after the conference.

The OFFIS Institute for Information Technology, founded in 1991, is an application-oriented non-profit research and development institute with close links to the Computer Science department of the University of Oldenburg in Lower Saxony, north-western Germany. Its primary mission is to adopt the findings from university basic research in computer science and other relevant disciplines, to stay in touch with new market demands through its many years of experience in co-operation projects with the industry, and to bridge the gap between “basic research” and “application demands” through application-oriented research. OFFIS staff currently counts about 250 employees. More than 150 scientists (in their vast majority computer scientists, but also engineers, economists, physicists and from other disciplines as well) work in interdisciplinary teams. OFFIS focuses its R&D activities in three challenging application areas: Energy, Health, and Transportation.

**General Chair:**

**Frank Oppenheimer, OFFIS**

Frank Oppenheimer received his Diploma in 1997 and 2005 his PhD in Computing Science from the Carl v.Ossietzky University Oldenburg where he worked as researcher at the Department of Computing Science until 2001.

In late 2001 he became Manager of the System Design Methodology Group and in 2008 Director in the R&D division Transportation at the OFFIS - Institute for Information Technology. Since 2005 he is the Chair of the LBSD thematic area of the FDL conference and is reviewing member of several other program committees. Frank’s prime interests in research are hardware/software interface modelling, programming models for multicore/multiprocessor platforms and synthesis and design methods for heterogeneous, adaptive systems.
**Keynote Speakers**

**Harry Foster** is Chief Scientist for Mentor Graphics’ Design Verification Technology Division. He holds multiple patents in verification and has co-authored six books on verification - including the 2008 Springer book Creating Assertion-Based IP. Harry was the 2006 recipient of the Accellera Technical Excellence Award for his contributions to developing industry standards, and was the original creator of the Accellera Open Verification Library (OVL) standard. Harry chairs the IEEE-1850 Property Specification Language (PLS) working group.

**Gerald Holweg** was born in Graz, Austria, in 1960. He received his Masters degree (DI) in Electronic Engineering at the Graz University of Technology in 1983 and started his professional career as ASIC design engineer at AMI-Austria in October 1984. In 1995, he took the position of Development Manager for the product line Contactless Smart Cards at MIKRON, which joined PHILIPS in June 1995. In February 1998 he started working as Director of Development for Chip Card and Security IC’s at start-up Design Centre SIEMENS Entwicklungszentrum für Mikroelektronik in Graz, which changed to INFINEON Technologies Development Centre in 1999. Since 2003 he is responsible for Predevelopment Programs and Projects with focus on Contactless and RF Technologies.

**Steffen Müller** started his career 1993 at MAZ Microelectronic Application Centre, Hamburg. Joined 1997 Robert Bosch Multimedia Systems. He led the functional verification of the first one-chip DAB channel and source decoder and continued as project leader of a MOST / audio gateway chip development at Blaupunkt. Started in 2000 with Philips Semiconductors, today NXP Semiconductors. Held various department lead positions in the area of general design services, project and program management, and system development in consumer electronics, mainly Digital TV. He heads since end of 2008 the Systems & Applications In-Vehicle Networking activities within the automotive business where NXP Semiconductors is market leader.
Technical Area Chairs

**EAMS TA Chair: Prof. Christoph Grimm, TU Vienna**

Christoph Grimm received his Diploma in Electrical Engineering in 1994 from TU Darmstadt and his Ph.D. in Computer Science in 1999 from University of Frankfurt. He worked as post-doc at Universities of Frankfurt and Hannover. Since 2006 he is full professor for Embedded Systems at TU Vienna’s Institute of Computer Technology. Christoph Grimm’s research interest is design methodology of analog/mixed-signal systems and design of SoC for power management in future green homes. He contributed the development of IEEE 1076.1 (VHDL-AMS) and IEEE 1076.6 (VHDL-SWG). In 2001, was co-founder of the OSCI SystemC AMS study group. He serves the OSCI AMS WG as vice chair and contributed as co-author to the SystemC AMS 1.0 extensions standard and the SystemC AMS users’ guide.

Christoph Grimm has contributed to the major conferences as PC or SC member or chair. He is head of the scientific advisory board of OVE and of the Austrian Society for Microelectronic Systems, speaker of the research cluster “AutCom” of TU Vienna, and scientific advisor for microelectronic and automotive companies. He is member of IEEE, OVE, and VDE.

**LBSD TA Chair : Martin Radetzki, University of Stuttgart**

Martin Radetzki received the Dipl.-Inform. and Dr.-Ing. degrees in Computer Science from Oldenburg University in 1996 and 2000, respectively. From 2000 until 2005, he held industry positions as a design engineer and as a design methodology project manager. Since 2005, he has been a professor of Embedded Systems Engineering in the faculty of Computer Science and Electrical Engineering, University of Stuttgart, Germany. His research group contributes to the Cluster of Excellence on Simulation Technology, SimTech. His main research interests are in the fields of specification and design of embedded systems functionality and architecture and the corresponding aspects of system simulation and reliability.

**Julio Medina, University of Cantabria, UMES TA Chair**

Julio Medina is graduated as Electronics Engineer from the Universidad Nacional de Ingeniería, Perú, in 1987. He obtained the Master in Real-Time Systems (1993) and the Doctorate in Telecommunications Engineering (2005) from the Universidad de Cantabria, Spain. He developed electronics and embedded software for nuclear instrumentation in the Peruvian Nuclear Research Center, then worked as assistant professor in electronics instrumentation and software engineering, and did research on distributed real-time systems. During the doctorate period he concentrated on the modeling of real-time systems developed with object-oriented techniques, being later co-author of the UML Profile for MARTE of the OMG in a post-doctorate research at the Commissariat a l’Energie Atomique in France. Currently he is lecturer in the Universidad de Cantabria and does research in several European projects. His main research topics include the modeling of real-time distributed systems for schedulability analysis, the UML representation of such models, and its usage for modular and component-based development strategies.
**Program Committee**

**Assertion Based Design, Verification & Debug**

**TA Chair: Prof. Dominique Borrione, TIMA**
- El Mostapha Aboulhamid, University of Montreal
- Claudia Blank, Intel
- Eduard Cerny, Synopsys
- Emanuelle Encrenaz, University Paris 6
- Hans Eweking, University of Darmstadt
- Harry Foster, Mentor Graphics
- Franco Fummi, University of Verona
- Pierre Laurence, University of Grenoble
- Ashraf Salem, Ain Shams University
- Pablo Sanchez, University of Cantabria
- Julien Schmaltz, Radboud U. Nijmegen

**UML and MDE for Embedded System Specification & Design**

**TA Chair: Julio Medina, University of Cantabria**
- Gjalt De Jong, ArchWorks
- Robert de Simone, INRA Sophia-Antipolis
- Peter Green, UMIST, Manchester
- Leandro Soares Indrusiak, University of York
- Jan Jürjens, Fraunhofer ISST
- Marcello Mura, Lugano University
- Mauro Prevostini, Lugano University
- Ralf Seepold, HTWG Konstanz
- François Terrier, CEA
- Dragos Truscan, Åbo Akademi University
- Yves Vanderperren, EPO
- Jeroen Voeten, Eindhoven UT

**Language-Based System Design**

**TA Chair: Martin Radetzki, University of Stuttgart**
- Jean-Philippe Babau, INSA Lyon
- Tomas Bautista, IUMA Las Palmas
- Mladen Berekovic, U. of Braunschweig
- Axel Braun, University of Tuebingen
- Peter Flake, Elda
- Joachim Gerlach, U. of Albstadt-Sigmaringen
- Daniel Große, University of Bremen
- Christian Haubelt, U. of Erlangen-Nurnberg
- Fernando Herrera, University of Cantabria
- Lars Kruse
- Bernhard Niemann, Fraunhofer, IIS
- Hiren Patel, University of Waterloo
- Martin Radetzki, University of Stuttgart
- Ingo Sander, KTH Stockholm
- Sandeep Shukla, Virginia Tech
- Yves Vanderperren, EPO

**Embedded Analog and Mixed-Signal System Design**

**TA Chair: Prof. Christoph Grimm, TU Vienna**
- Martin Barnasconi, NXP Semiconductors
- Ernst Christen, Synopsys
- Umberto Gatti, Nokia-Siemens
- Joachim Haase, FhG IIS/EAS Dresden
- Jan Haase, TU Vienna
- Lars Hedrich, University of Frankfurt
- Egbert Molenkamp, University of Twente
- Guido Schreiner, MathWorks
- Serge Scotti, STMicroelectronics
- David W. Smith, University of Southampton
- Karsten Einrich, FhG-IIS/EAS
- Marie-Minerve Louerat, UPMC
- Alain Vachoux, EPFL
- Tom Kazmierski, University of Southampton
- Chris Myers
- Alan Mantooth
- Karsten Einwich
- Marie-Minerve Louerat
- Alain Vachoux
- Tom Kazmierski
- Chris Myers
- Alan Mantooth
- Karsten Einwich
- Marie-Minerve Louerat
- Alain Vachoux
- Tom Kazmierski
- Chris Myers
- Alan Mantooth
Conference Scope
FDL is an international forum to exchange experiences and promote new trends in the application of languages, their associated design methods and tools for the design of electronic systems. The Forum is organized around four Thematic Areas (TA) described below and includes working sessions, poster sessions, embedded tutorials, panels and technical discussions. Industrial Workshops and Fringe Meetings such as user group or standardization meetings are also held in conjunction with the Forum.

ABD TA: Assertion Based Design, Verification & Debug
TA Chair: Dominique Borrione, TIMA
The ABD Thematic Area welcomes research contributions, tool demonstrations, reports on standardization activities and effective applications in all aspects of innovative property expression and processing, with an emphasis on frontier design levels, verification, automatic synthesis and mechanized debug aids. The assertion of formal properties provides a uniform expression of expected system behavior, or constraints that are assumed on the environment, for a variety of design tasks: verification of functional correctness, generation of test stimuli, synthesis of observation monitors and on-line tests, model checking on the reachable state space, direct synthesis from assertions, etc. Standardized formalisms such as PSL and SystemVerilog assertions were initially intended for synthesizable RTL; their application is now considered at transaction levels and for mixed system designs.

LBSD TA: Language-Based System Design
TA Chair: Martin Radetzki, University of Stuttgart
The LBSD TA addresses language-based modelling and design techniques for simulation, debugging, transformation, and analysis of digital hardware/software embedded systems. Contributions are welcome on innovative applications, language or library design, and methodological aspects. SystemC will undergo restandardization to keep up to date with users' needs. Hence, contributions on new applications and evolution of SystemC are highly welcome. Equally welcome are papers dealing with SystemVerilog, functional languages, UML in conjunction with executable specification, and emerging languages. Aspects of methodology, interoperability, simulation semantics, and models of computations will find an audience just like embedded software modelling techniques and technology or domain specific approaches, e.g. for signal processing applications or reconfigurable computing platforms. Moreover, transaction level modelling (TLM) with any language, IP-based system design (e.g. IP-XACT), modelling aspects in system synthesis, innovative industrial case studies, and efficient parallel simulation of high-level models are in scope.

EAMS TA: Embedded Analog and Mixed-Signal System Design
TA Chair: Christoph Grimm, TU Vienna
The EAMS TA addresses design, modeling, and verification of heterogeneous systems that include significant part of "analog" or "continuous" behavior such as cyber physical systems, wireless sensor networks, and of course analog/mixed-signal circuits. A new challenge is the tight interaction of analog or physical components with - maybe distributed - digital hardware/software systems. Topics of interest include specification, modeling, simulation, (symbolic) analysis, verification, design, (virtual) prototyping, and synthesis of analogue, mixed-signal, and mixed-technology systems, wireless sensor nets, and cyber physical systems. Focus of contributions should be on languages, models, representations, and tools such as VHDL-AMS, SystemC-AMS, Modelica, Matlab/Simulink, etc. The EAMS TA aims at presenting research activities, design experiences, and standardization issues related to these topics.

UMES TA: UML and MDE for Embedded System Specification & Design
TA Chair: Julio Medina, University of Cantabria
Model driven methods, mostly based on the Unified Modelling Language, increasingly support semi-formal methods for system level design of complex embedded systems including multi-core, highly programmable platforms and heterogeneous Systems-on-Chip. UMES related research topics in this field are Executable UML, model driven development, model transformations, UML semantics, meta-modelling, e.g., for SystemC and other System Description Languages or HDLs, UML profiles, e.g. SysML, MARTE, UML for SoC, and formalization of UML towards domain specific languages for simulation and synthesis. Other welcomed topics are standardization work, modelling languages for real-time and embedded systems, model driven techniques for performance analysis, validation and verification, SDL, AADL, OCL, XMI, and practical design experiences with UML or in general model driven engineering (MDE) approaches.
Abstract
In the fall of 2010, Wilson Research Group was commissioned to conduct an industry wide, blind study focused on functional verification. This study was one of the largest electronic functional verification studies ever conducted. A number of interesting observations emerged from the study, such as: (a) reuse adoption is increasing, (b) the effort spent in functional verification is increasing, (c) the industry in its adoption of advanced functional verification techniques. This keynote presents data highlights and analysis from the Wilson Research Group study covering a wide range of topics and trends from physical aspects of design, to various verification methodology adoption, to design and verification language adoption.
**Abstract**

This session includes presentations that deal with design and optimization of complex, heterogeneous systems such as wireless sensor networks or cyber-physical systems. The first paper describes a method for analyzing and optimizing power consumption at application level. The second paper describes combination of SystemC AMS and TLM extensions to model a CMOS Video Sensor. The third paper describes modelling of a satellite network.

*Designing Low-Power Wireless Sensor Networks*
   Joseph Wenninger, Javier Moreno, Jan Haase, and Christoph Grimm (Vienna University of Technology)

*Behavioral Modeling of a CMOS Video Sensor Platform using SystemC AMS / TLM*
   Fabio Cenni, Serge Scotti (ST Microelectronics) and Emmanuel Simeu (TIMA Laboratory)

*SystemC-AMS Model of a Dynamic Large-Scale Satellite-Based AIS-Like Network*
   Mu Zhou and Rene Van Leuken (Delft University of Technology)

---

**Co-session 1 – Tutorial:**

**High Level Synthesis: From C++ to VHDL – Part 1**

By CoSynth, Oldenburg, Germany, www.cosynth.com
organisers: Christian Stehno, Henning Kleen and Andreas Herrholz

Over the last years, a number of development tools for a new hardware design paradigm, which can be summarized as *Electronic System Level* design, have emerged and established within the market. They lift the existing manually driven HDL based process to a design flow with C/C++ and SystemC based entries.

In this tutorial, we will summarize the major advantages of such high level design processes and present the general steps of such a process based on an example design. The most crucial component of this process is the synthesis tool. It automates the conversion from high-level descriptions to hardware designs. Another important aspect is the integration of these synthesis results into a complete system design.

The tutorial uses the running example of a hardware accelerated video filter chain. The requirements and development steps for system level design are discussed. The whole design process, from an initial C++ implementation to the final IP core, is shown. A special focus is put on the refinement of the SystemC virtual platform into a synthesizable representation. This code is then transformed into VHDL utilizing the CoSynth Synthesizer tool. The necessary coding guidelines and typical restructuring measures of the code are detailed in several examples. The synthesis result is next integrated into an existing FPGA-based system with camera and display interfaces. Using the Xilinx EDK, the IP core and platform are integrated into a running design for the Virtex-5 architecture.
**Session 2 – EAMS, Part 2: Circuit Modelling and Design**

*Chair: Alain Vachoux, EPFL*
*Co-Chair: Torsten Mähne, Université Pierre et Marie Curie, LIP6 Laboratory*

**Abstract**

The session presents aspects of circuit modelling and design. The first paper discusses the linking of circuit and system design by appropriate behavioral models. The second one is about modelling new, emerging devices: Graphene FET. The third paper deals with systematic specification of analog circuit properties to enable verification and synthesis.

*Abstract Modeling and Estimation of a High Performance Tobey’s PGA*
Sumit Adhikari, Christoph Grimm and Jan Haase (Vienna University of Technology)

*VHDL-AMS Model of a Dual-Gate Graphene FET*
Ime Umoh and Tom Kazmierski (University of Southampton)

*A Machine-Readable Specification of Analog Circuits for Integration into a Validation Flow*
Mingyu Ma, Lars Hedrich and Christian Sporrer (University of Frankfurt)

---

**Co-session 2 – Tutorial:**

High Level Synthesis: from C++ to VHDL – Part 2

By CoSynth, Oldenburg, Germany, [www.cosynth.com](http://www.cosynth.com)
Organisers: Christian Stehno, Henning Kleen and Andreas Herrholz
Panelists
Kerstin Eder, University of Bristol, England
Franco Fummi, University of Verona, Italy
Laurence Pierre, TIMA Laboratory, University of Grenoble, France
Laurent Maillet-Contoz, STMicroelectronics, Grenoble, France (tbc)

Abstract:
System design has traditionally been partitioned into multiple, independent development domains (for example, electrical, mechanical, and software), where each domain maintains its own design and verification description languages, methodologies, and tools. Yet, as more emphasis is placed on early system analysis, prior to partitioning and refinement, traditional system design approaches have proven to be problematic. It has been suggested that properties might provide a formal mechanism for unifying today's system design process. As attractive as this might seem, there are still many unanswered process questions. For example, are today's property languages expressive enough for capturing properties that then can be used at all levels of abstraction—or will new languages be required? Does the design refinement process impose any restrictions on the types of properties that can be reused? What are the main problems that need to be solved? This esteemed panel of experts will explore the challenges and opportunities afforded a property-driven, system design process.
European SystemC Users’ Group Meeting
Chair: Axel Braun, Tübingen University
Co-Chair: Wolfgang Rosenstiell, FZI

Agenda

16:00: OSCI Section:
OSCI News and Update

16:20: SystemC User Presentations:

- Advancing the SystemC Analog/Mixed-Signal (AMS) extensions
  Univ.Prof. Dr. Christoph Grimm (Vienna University of Technology)

- An Advanced Constrained Random Verification Environment for SystemC
  Daniel Große, Finn Haedicke, Hoang M. Le, Rolf Drechsler (University of Bremen, Germany)

- Non-intrusive TLM-2.0 Transaction Observation, Interception, and Augmentation
  Philipp A. Hartmann, Maher A. Fakih, Kim Grüttner (OFFIS Institute for Information Technology, Oldenburg, Germany)

- High Level Synthesis Methodologies and Tools
  Christian Stehno (CoSynth GmbH & Co. KG)

18:15: Reception & Refreshments

The European SystemC Users Group Meeting is supported by ECSI, the Open SystemC Initiative, and these Global Sponsors:
ARM, Cadence, Forte, Synopsys, Mentor Graphics, Xtreme EDA

www.systemc.org
Abstract:
One of the most emerging fields is the development of smart, miniaturized, ultra-low power systems for parameter monitoring and control in different application domains, e.g. environmental monitoring, structural health monitoring in the automotive and aeronautic field, telemedical applications, tracking of goods and smart power grid control, just to name a few. The presenter discusses how semiconductor devices enable the way to a successful roll-out scenario.
Session 3 – ABD, Part 1:
Assertion-Based Technology for Verification and Synthesis
Chair: Ashraf Salem, Ain Shams University

Abstract
This session is devoted to assertion-based verification. The first paper addresses the automatic derivation of simulation stimuli that satisfy the activation condition of an assertion. The second paper discusses the addition of asynchronous monitors to clocked design, for online detection of timing faults in the presence of varying operating conditions. The last paper describes the automatic extraction of RTL assertions from behavioral descriptions and specifications during the high level synthesis, to enable assertion-based verification of the synthesized design.

Improvement of Assertion-Based Verification through the Generation of Proper Test Sequences
Laurence Pierre and Laila Damri (TIMA - CNRS-GrenobleINP-UJF)

Does Asynchronous Technology Bring Robustness in Synchronous Circuit Monitoring?
Alexandre Porcher, Katell Morin-Allory, Laurent Fesquet (TIMA), and Alejandro Chagoya (CIME Nanotech)

Assertion Support in High-Level Synthesis Design Flow
Aurélien Ribon, Bertrand Le Gal, Christophe Jego, and Dominique Dallet (University of Bordeaux)

Wednesday, September 14, 2011
11:00-12:30
Room: E02

Co-Session 3 – LBSD, Part 1:
Syntactic Sugar? - Language Design and Semantics
Chair: Daniel Große, University of Bremen
Co-Chair: Frank Oppenheimer, OFFIS

Abstract
System designers and tool developers benefit from the use of languages with productivity-enhancing features and clearly defined semantics. This session features a presentation of TDHL++, a VHDL extension that offers advanced templating and object-orientation. The second paper presents a semantics of transaction level models (TLMs) that allows capturing non-deterministic timing as introduced by techniques such as temporal decoupling. Two short presentations elaborate on solutions to intricacies of synchronous language semantics and on a generic TLM execution model for fast simulation.

Bringing C++ Productivity to VHDL World: from Language Definition to a Case Study
Ivan Shcherbakov, Christian Weis and Norbert When (TU Kaiserslautern)

A Metamodel and Semantics for Transaction Level Modeling
Rauf Salimi Khaligh and Martin Radetzki (University of Stuttgart)

Schizophrenia and Causality in the Context of Refined Clocks (short presentation)
Mike Gemünde, Jens Brandt and Klaus Schneider (TU Kaiserslautern)

A Generic Execution Model for Efficient Performance Evaluation of System Architectures at Transaction Level (short presentation)
Sebastien Le Nours, Anthony Barreteau and Olivier Pasquier (University of Nantes)
Abstract: This session offers two well described academic approaches and one industrial experience addressing different parts of the model based validation and verification problems. The first proposes a framework to include model based testing in the domain of very constraint embedded systems, the second includes static validation at transaction level using OCL rules plus the verification of the expected behavior using dynamic validation of sequence charts. The third uses UML models in the design of an IP based TDMA radio protocol, and includes component wrapper code generation on an execution platform, automatic tests generation from the components behaviors specification, and non-functional analysis.

Integrated Model-Based Approach and Test Framework for Embedded Systems
Padma Iyenghar and Elke Pulvermueller (University of Osnabueck)
Clemens Westerkamp and Juergen Wuebbelmann (UAS, Osnabrueck)

A UML Based Framework for Efficient Validation of TLM 2 Models
Vaibhav Jain, Anshul Kumarand, and Preeti Ranjan Panda (Indian Institute of Technology Delhi)

Invited Industrial Experience Report:
Experiments on the Analysis from a Radio Protocol Application Modeling
Michel Bourdellès, François Dupont, Fabien Peureux, Thomas Vergnaud, and Shuai Li
Session 5 – UMES, Part 2: MARTE at Work & Standardization Trends
Chair: Julio Medina, University of Cantabria
Co-Chair: Gjalt de Jong, ArchWorks

Abstract: This session presents two approaches that map the IP/XACT standard to UML plus MARTE. The first addresses the generation of platform models as formalisms for the validation. The second studies the dynamic partial reconfiguration of FPGA designs, trying to exploit the reuse of IPs in a model based approach. The MARTE Users Group meeting will present current standardization trends at the OMG.

A Framework for the Generation from UML/MARTE Models of IP-XACT HW Platform Descriptions for Multi-Level Performance
Fernando Herrera and Eugenio Villar (University of Cantabria)

IP-XACT and MARTE Based Approach for Partially Reconfigurable Systems-on-Chip
Gilberto Ochoa, El-Bay Bourennane, Ouassila Labbaniand, Kamel Messaoudi
(LE2I Laboratory, Université de Bourgogne)

Colocated Meeting: MARTE Users Group
Current Standardization Trends: Towards an RFP for A Precise Semantics of UML Composite Structures

Co-Session 5 – LBSD, Part 2: Hurry up! - Speedy Simulation Techniques
Chair: Eugenio Villar, University of Cantabria
Co-Chair: Robert Wille, University of Bremen

Abstract: Simulation of large digital systems requires high performance to enable extensive design space exploration through quick turn-around times. SystemC data types are known to slow down simulation significantly, compared to plain C types. A new library of efficient data types with bit-true modelling support is covered by the first presentation. The second paper shows how the principle of message-based parallel discrete event simulation can speed up simulation of transaction level modelling even in a sequential simulation scenario. The efficiency of system level design techniques in improving design processes is investigated with the help of process simulation by the third contribution.

Efficient Implementation and Abstraction of SystemC Data Types for Fast Simulation
Nicola Bombieri, Franco Fummi, Valerio Guarnieri, Francesco Stefanni, and Sara Vinco (U. of Verona)

A Case Study on Message-Based Discrete Event Simulation for Transaction Level Modeling
Bastian Haetzer and Martin Radetzki (University of Stuttgart)

Impact Simulation of Changes to Development Processes: An ESL Case Study
Frank Poppen, Roland Koppe, Kim Grüttnner (OFFIS), and Axel Hahn (University of Oldenburg)
Abstract

New regulations on CO2 emission has been introduced and led to discussions between car makers, module makers, and semiconductor suppliers. Development programs have been set up on electro-mobility that influences automotive research activities and requirements for the electronics. The electrical vehicle is not a new invention but received new attention because recent results in battery technology, drive efficiency, and energy management are promising. Both, conventional car and electrical vehicle, share the need to save energy despite increasing electronic content to keep CO2 tax and operation range in an acceptable order for end-users. The trend in microelectronics goes to more integration, less power consumption, better EMC robustness, and more chip complexity. The example is In-vehicle Networking and here the development of System-Basis Chips, the integration of periphery of the microcontroller in an electronic control unit. Higher complexity of the system and its application shows the need for virtual prototyping that brings digital, analog, and software elements together at an early stage of the chip development. A design example and its virtual prototyping approach will be shown.
Abstract
Eventually, systems modelled at high levels of abstraction must be refined towards an implementation. The first paper shows how language features that describe control flow can be synthesized efficiently as reversible logic circuits. The second contribution deals with the mapping of adaptive processes onto dynamically reconfigurable hardware. Two short presentations deal with a systematic description of system-level refinements based on the ForSyDe model and with dynamic scheduling of high-level descriptions for incorporating the impact of hardware synthesis in system-level simulations.

Efficient Realization of Control Logic in Reversible Circuits
Sebastian Offermann, Robert Wille and Rolf Drechsler (University of Bremen)

SystemC Refinement of Abstract Adaptive Processes for Implementation into Dynamically Reconfigurable Hardware
Fernando Herrera and Eugenio Villar (University of Cantabria), Philipp A. Hartmann (OFFIS)

Semi-Formal Refinement of Heterogeneous Embedded Systems by Foreign Model Integration (short presentation)
Seyed Hosein Attarzadeh Niaki and Ingo Sander (KTH Royal Institute of Technology)

Hardware Performance Estimation by Dynamic Scheduling (short presentation)
Pablo González De Aledo Marugán, Javier González-Bayón, and Pablo Sanchez (U. of Cantabria)
Abstract
Modelling of systems and evaluation of system models are key techniques that support first-time-right design. The first paper presents a new modelling technique for integrating heterogeneous models of computation. Evaluation of power and performance trade-offs in system-level design are addressed by the second contribution. The third presentation covers an approach for early dependability analysis based on SystemC transaction level models.

Integrating System Descriptions by Clocked Guarded Actions
Jens Brandt, Mike Gemünde and Klaus Schneider (University of Kaiserslautern)
Sandeep Shukla (Virginia Tech) and Jean-Pierre Talpin (INRIA)

ESL Power and Performance Estimation for Heterogeneous MPSoCs Using SystemC
Martin Streubühr, Rafael Rosales, Jürgen Teich (University of Erlangen-Nuremberg),
Ralph Hasholzner (Intel Mobile Communications) and Christian Haubelt (University of Rostock)

Analyzing Dependability Measures at the Electronic System Level
Marc Michael, Daniel Grosse and Rolf Drechsler (University of Bremen)
The COMPLEX (COdesign and power Management in PLatform-based design space EXploration) consortium develops a new design environment for platform-based design-space exploration offering developers of next-generation mobile embedded systems a highly efficient design methodology and tool chain. The integrated environment allows iterative exploration and refinement of advanced applications to meet market requirements. The design technology in particular enables fast simulation and explores the use of different implementations at Electronic System Level (ESL) with up to bus-cycle accuracy at the earliest instant in the design cycle. The main objectives are:

- Highly efficient and productive design methodology and holistic framework for design space exploration of embedded HW/SW systems.
- Combination and augmentation of well-established ESL synthesis & analysis tools into a seamless design flow enabling performance & power aware virtual prototyping of the HW/SW system.
- Interfacing next-generation model-driven SW design approach and industry standard model-based design environments.
- Multi-objective co-exploration for assessing design quality and optimizing the system platform with respect to performance, power, and reliability metrics.
- Fast simulation and assessment of the platform at ESL with up to bus-cycle accuracy at the earliest instant in the design cycle.
- Optimization benefits from run-time mode adaptation techniques, such as dynamic power management or application adaptation to varying workloads.

COMPLEX related papers presented at FDL 2011:

**Session UMES2, Wednesday, September 14, 16:00-17:30**
A Framework for the Generation from UML/MARTE Models of IP-XACT HW Platform Descriptions for Multi-Level Performance
Fernando Herrera and Eugenio Villar (University of Cantabria)

**Session LBSD2, Wednesday, September 14, 16:00-17:30**
Impact Simulation of Changes to Development Processes: An ESL Case Study
Frank Poppen, Roland Koppe, Axel Hahn and Kim Grüttner

**Session LBSD3, Thursday, September 15, 11:00-12:30**
SystemC Refinement of Abstract Adaptive Processes for Implementation Into Dynamically Reconfigurable Hardware
Fernando Herrera, Eugenio Villar and Philipp A. Hartmann

**ESCUG Meeting, Tuesday, September 13, 16:00-18:30**
Non-intrusive TLM-2.0 Transaction Observation, Interception, and Augmentation
Philipp A. Hartmann, Maher A. Fakih, Kim Grüttner

A poster session will be organized at FDL to present COMPLEX objectives and current results.
Languages for Embedded Systems and their Applications
Selected Contributions from FDL ‘08
Radetzki, Martin (Ed.)
2009, XIV, 326 p., Hardcover

Advances in Design and Specification Languages for Embedded Systems
Selected Contributions from FDL’06
Huss, Sorin A. (Ed.)
2007, X, 358 p., Hardcover

Design and Specification Languages for SoCs
Selected Contributions from FDL’04
Boulet, Pierre (Ed.)
2005, X, 305 p., Hardcover

Embedded Systems Specification and Design Languages
Selected Contributions from FDL’07
Villar, Eugenio
2008, X, 278 p., Hardcover

Applications of Specification and Design Languages for SoCs
Selected papers from FDL’05
Vachoux, Alain. (Ed.)
2006, XXII, 312 p., Hardcover

Purchase your FDL books and more at www.ecsi.org!
Welcome to Oldenburg

Welcome to Oldenburg - the Übermorgen. Übermorgen means the day after tomorrow, and Oldenburg has chosen this label to express that it is firmly rooted in the future. Oldenburg is home to 160,000 people and the economic hub of the Bremen - Oldenburg metropolitan region. It is a university city and was the German City of Science in 2009. A former princely residence, it looks back over a history spanning 1,200 years. Oldenburg is a lively city with a great deal of charm embedded in a beautiful, unspoilt natural landscape.

Language

The language of the conference will be in English.

Location

OFFIS e.V.
Escherweg 2
26121 Oldenburg
Rooms E02 & F02

Conference Hours

Conference/Registration Hours:
- Monday 9:00 – 17:30
- Tuesday 9:00 – 17:30
- Wednesday 9:00 – 16:00

Social Event

The 2011 FDL Social Event will start with a guided tour of the State Museum of Natural History in Oldenburg, featuring a special exhibition about the moor, which is one of the historically distinct landscapes in this area. Following the museum, we will have dinner in the stately Fürstensaal, at the restaurant Klinkerberg.

Contact Information

Dr. Adam Morawiec
ECSI Director
ECSI, Electronic Chips & Systems design Initiative
Parc Equation - 2 avenue de Vignate
38610 Gières, France
Tel: +33 4 76 63 49 34, Fax: +33 9 58 08 24 13
office@ecsi.org

www.ecsi.org