The „FIRSTs“ by the Xputer Lab

Reiner Hartenstein[1] (R. H.), TU Kaiserslautern, July 2017

The Anti-Machine Paradigm (“Xputer”), counterpart of the von Neumann paradigm by using data counters instead of a program counter [1]. Running data streams instead of instruction streams. To cope with the von Neumann Syndrome we urgently need this alternative machine paradigm. Data sequencers instead of an instruction sequencer: [2,3].

[1] N. N.: Xputer-related Literature; TU Kaiserslautern, 2015 <pdf>, pt.2: <pdf>

[2] R. H., A. G. Hirschbiel, M. Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; InfoJapan'90 - memorating the 30th Anniversary Computer Society of Japan, Tokyo, Japan, 1990 <pdf>

[3] Invited Reprint: in Future Generation Computer Systems 7 1991/92 <pdf>

[4] R. H.: High Performance Machine Paradigm based on Auto-sequencing Data Memory; HICSS 24th Hawaii Int'l Conf. on System Sciences, January 1991, Koloa, Hawaii, <pdf> <pdf2> <pdf3> <pdf4>

[5] R. H., H. Reinig, M. Riedmüller, K. Schmidt: A Novel Computational Paradigm: Much More Efficient Than von Neumann Principles; The 13th IMACS World Congress, Dublin Ireland, July 1991, <pdf>

[6] R. H., K. Schmidt, H. Reinig, M. Weber: A Novel Compilation Technique for a Machine Paradigm Based on Field-Programmable Logic; FPL International Conference on Field Programmable Logic and Applications, Oxford 1991 <pdf>

[7] Karin Schmidt: Xputer - eine Alternative zum Computer? - Innovatives Hochleistungs-Rechner-prinzip aus Kaiserslautern; UNI SPECTRUM, Technische Universität Kaiserslautern, Juli 1990 <pdf>

Generalization of the Systolic Array; Super-systolic array or Kress Array by introducing a new synthesis method and integrating auto-sequencing data memory (AsM) – adapting it into the Xputer paradigm

[8] R. H., R. Kress: A Datapath Synthesis System for the Reconfigurable Datapath Architecture; Asia and South Pacific Design Automation Conference, ASP-DAC'95, Makuhari, Chiba, Japan, August/September 1995 <pdf> <ppt>

[9] R. H., M. Herz, Th. Hoffmann, U. Nageldinger: "KressArray Xplorer: A New CAD Environment to Optimize Reconfigurable Datapath Array Architectures"; The 5th Asia and South Pacific Design Automation Conference (ASP-DAC 2000), Pacifico, Yokohama, Japan, Jan 25-28, 2000. <pdf>

[10] R. H.: "Generalization of the Systolic Array"; memo, TU Kaiserslautern, Oct 2003 <pdf>

[11] R. H.: KressArray: what's the achievement? Generalize the Systolic Array; Memo, TU KL'13 <pdf>

[12] R. H.: Karl Steinbuch about how to invent something; Memo, Nov. 2014 <pdf>

First Data-procedural Programming Language. In 1993 introducing ***the first data-procedural programming language*** (**MoPL**: Map-oriented Programming Language) supporting the Xputer machine paradigm (w. data counters instead of a program counter): ***for programming data streams instead of instruction streams*** (Flowware instead of Software).

[13] R. H., A. Ast, J. Becker, R. Kress, H. Reinig, K. Schmidt: MoPL-3: A New High Level Xputer Programming Language; subm. to 3rd Int'l FPL Workshop, Oxford, UK, Sept. 1993 <pdf>

[1] Full Professor TU Kaiserslautern, Adjunct Professor KIT Karlsruhe, IEEE life fellow, FPL fellow, SDPS fellow

[14] R. H., A. Ast, J. Becker, R. Kress, H. Reinig, K. Schmidt: Data-procedural Languages for FPL-based Machines; 4th FPL Workshop (FPL'94), Prague, Sep 7-10 1994, <pdf>

Reconfigurable Computing Compiler [15] R. H. et al.: <pdf>

FPGA usage for saving energy, [16] R. H. (keynote address): "Reconfigurable computing means to brave the paradigm chasm"; The HiPEAC Workshop on Reconfigurable Computing, Gent, Belgium, January 28, 2007 <pdf>

[17] R. H.: Are Supercomputers an Endangered Species? <pdf>

[18] R. H.: contrib. to panel "Flexibility and Low Power; a Contradiction in Terms? panelists: Peter Wintermayr (moderator), Reiner Hartenstein, Heinrich Meyr, and Steve Leibson; The 8th Symp. on Low Power Electronics and Design 2006 (ISLPED), Oct. 2006, Tegernsee, Germany <pdf>

Re-definition of low power design for HPC: a paradigm shift

[19] R. H. (conference opening keynote): The Redefinition of Low Power Design for HPC: a Paradigm Shift; 21st Symp. on Microelectronic Technology and Devices (SBMICRO 2006), Aug 28 - Sep 1, 2006, Ouro Preto, MG, Brasil <pdf>

The Generic Address Generator (GAG); <Figure 1> [20] (invited paper): Michael Herz, Reiner Hartenstein, Miguel Miranda, Erik Brockmeyer, Francky Cathoor: Memory Addressing Organization for Stream- based Reconfigurable Computing; The 9th IEEE International Conference on Electronics, Circuits and Systems - ICECS 2002, September 15-18, 2002, Dubrovnik, Croatia <pdf>

[21] R. H., A. G. Hirschbiel, M. Riedmüller, K. Schmidt, M. Weber: A High Performance Machine Paradigm Based on Auto-Sequencing Data Memory; HICSS-24, Hawaii Int'l Conf. of System Sciences, Koloa, Hawaii, 1996 <pdf>

[22] R. H., A. Hirschbiel, M. Weber: The Machine Paradigm of Xputers and its Application to Digital Signal Processing Acceleration; 1990 International Conf. on Parallel Processing (ICPP 90), August 1990, St. Charles, Illinois, USA, <pdf>

[23] R. H., A. Hirschbiel, M. Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; CONPAR '90 - VAPP IV, Sep 1990, Zürich, Switzerland <pdf>

[24] R. H. (invited presentation): Reconfigurable Computing Development - - Trends; Dot Wireless Inc., San Diego, CA, USA, 1999 <pdf>

The Shuffle Sort Algorithm [25] R. H., K. Bastian, W. Nebel: „VLSI-Algorithmen: innovative Schaltungstechnik statt Software - SHUFFLE SORT: VLSI-Beispiel eines Sortierers; Ges. f. Meß- und Regelungstechnik: Tagung Mikroelektronik in der Automatisierungstechnik, Baden-Baden 1985; VDI-Bericht <pdf>

[26] Martin Duhl: Die schrittweise Entwicklung und Beschreibung einer Shuffle-Sort-Array Schaltung in HYPERKARL aus der Algorithmischen Darstellung des BUBBLE-SORT-ALGORITHMUS, Projektarbeit, TU Kaiserslautern 1986 <copy>

[27] R. H.: "The Shuffle Sort Algorithm; Memo, TU Kaiserslautern, Nov 2013 <pdf>

KARL Hardware Description Language

[28] R. H.: The world-wide dominant hardware description language throughout the 80ies; <html>
[29] R. H.: The KARL System (Summary); <pdf>
[30] R. H.: KARL Users; <html>
[31] R. H.: 93 KARL Licensee Sites; <html>
[32] R. H.: KARL pages (a survey); <html>
[33] R. H.: ***Why did KARL disappear much later ?*** <html>

[34] R. H.: KARL-related literature <html>
[35] R. H.: KARL-related Quotation Index <html>
[36] R. H.: Major microchip designs implemented in using KARL and ABLED <html>

ABL Graphic Blockdiagram language, ……

[37] R. H.: Description of wiring patterns;
[38] R. H.: Domino notation; Wiki about domino notation;

Introducing Mead-&-Conway to the continent (EurAsia)

[39] R. H.: Das E.I.S.-Projekt und andere EDA-Ergebnisse; <html>
[40] R. H.: The E.I.S. Project and other EDA Achievements; <html>

Automatic VLSI Synthesis by Term Rewriting

[41] R. H.: Automatic VLSI Synthesis by top-down Term Rewriting (TR); <html>; The axioms; Multiplier bit generation; Description of the multiplier;

The world-wide first complete VLSI synthesis environment

[42] R. H.: The CVT Software Package around KARL and ABL; <Fig.33>

FFT on Xputer

[43] R. H., A. Hirschbiel, M. Weber: The Machine Paradigm of Xputers and its Application to Digital Signal Processing Acceleration; 1990 Int'l Conf. on Parallel Processing (ICPP 90), August 1990, St. Charles, Illinois, USA, <pdf>

[44] R. H., A. Hirschbiel, M.Weber: A Novel Paradigm of Parallel Computation and its Use to Implement Simple High Performance Hardware; CONPAR '90 - VAPP IV, Sep 1990, Zürich, Switzerland <pdf>

KressArray: the Generalization of the Systolic Array

[45] R. H.: Karl Steinbuch about how to invent something; <pdf>

Deficits in Reconfigurable Computing Education

[46] R. H. (workshop series opening keynote address): Reconfigurable HPC: torpedoed by Deficits in Education? Workshop on Reconfigurable Systems for HPC (RHPC); July 21, 2004, held in conjunction with HPC Asia 2004, 7th International Conference on High Performance Computing and Grid in Asia Pacific Region, Omiya Sonic City, Tokyo Area, Japan, July 20 - 22, 2004 <keynotes> <HPCAsia> <RHPC> <PDF> <PDF2>

Founder of the first international conference series about Reconfigurable Computing Education

[47] RCedu page: <html>

[48] R. H. (workshop opening keynote): Why we need Reconfigurable Computing Education; 1st Int'l Workshop on Reconfigurable Computing Education (RCedu) March 1, 2006, Karlsruhe, Germany <pdf1> <pdf2>

Founder of the first international conference series about energy-efficient computing

[49] R. H.: The PATMOS Page; <html>

[50] R. H.: The History of the International Workshop on Power And Timing Modeling Optimization and Simulation (PATMOS); <html>

Fighting against Corruption within ACM (and IEEE)

[51] R. H.: Conferences, Books & Periodicals on FPGAs & Reconfigurable Computing - proving that the official ACM perspective is wrong; <html>

Coined the Terms:

Domino Notation, Xputer, Configware, Flowware, Morphware, Generic Address Generator (GAG), Structured Hardware Design, Structured VLSI Design, KressArray, Auto-sequencing Memory (AsM), Auto-sequencing Data Memory (AsDM), <pdf>