CV of Reiner Hartenstein

Credited to be „The father of Reconfigurable Computing" (also pre-FPGA era) [1]

Creator of **KARL**[2], worldwide most successful [3] trailblazer HDL before VHDL

EU grant (80ies): ***85 mio ECU*** (pre-€) for complete **EDA framework** [4,5] **around KARL**

1981: visiting professor at UC Berkeley (& cooperation with Xerox PARC)

1983: founder of the German contribution to the Mead-&-Conway VLSI design revolution: the multi university „**E.I.S. project**" (federal gov. grant: ***38 million Deutschmark***)

Founder and co-founder of several international annual conference series

IEEE fellow, SDPS fellow, FPL fellow, best paper awards and other awards

Professor (ordinarius emeritus), TU Kaiserslautern

reiner@hartenstein.de

All acad. degrees from KIT Karlsruhe Institute of Technology (mentor: Karl Steinbuch)

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[1] qu. Viktor Prasanna (with Gerald Estrin as the grandfather of Reconfigurable Computing, who proposed it in 1960 WJCC)

[2] R. Hartenstein: Fundamentals of Structured Hardware Design; American Elsevier, 1977 -- **textbook bestseller**

[3] for a list of users, usage details, quotations and other info, see: http://www.fpl.uni-kl.de/staff/hartenstein/KARLUsers.html

[4] R. Hartenstein: The History of KARL and ABL; in: J. Mermet (editor): Fundamentals and Standards in Hardware Description Languages; ISBN 0-7923-2513-4, Kluwer (now Springer), September 1993. also see: http://xputers.informatik.uni-kl.de/karl/karl_history_fbi.html

his hobby: giving keynotes http://hartenstein.de/keynotes.htm

[5] format-checking functional floorplan graphic editor, and textual editors, calculus-based term rewriting floorplan generator, embedded router, automatic test generation, testability analysis, structured logic synthesis, simulator, et al. -- also see [4]