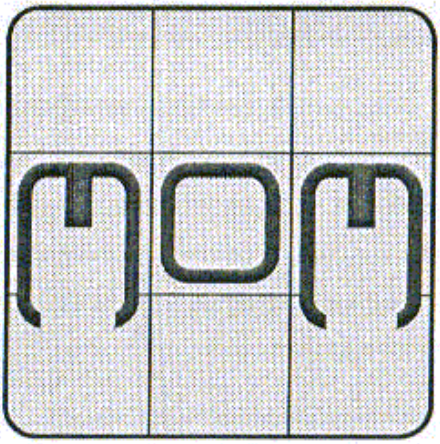


MOM - Map Oriented Machine

R. W. Hartenstein
A.G. Hirschbiel
M. Weber

Forschungsgruppe für Rechnerstrukturen und Technische Informatik
(Research Group on Computer Structures and Design Sciences)
Kaiserslautern University
Fachbereich Informatik
(Computer Science Department)
P.O. Box 3049
D-6750 Kaiserslautern, F.R.G.

phone : +49 (631) 205 - 2606
home: +49 (7251) 3575 or: +49 (6306) 545
telefax : +49 (631) 205 -3200
telex : 04 - 5627 unikl d
e-mail : abakus%uklirb@unido.uucp

Kaiserslautern, May 1989

The Problem

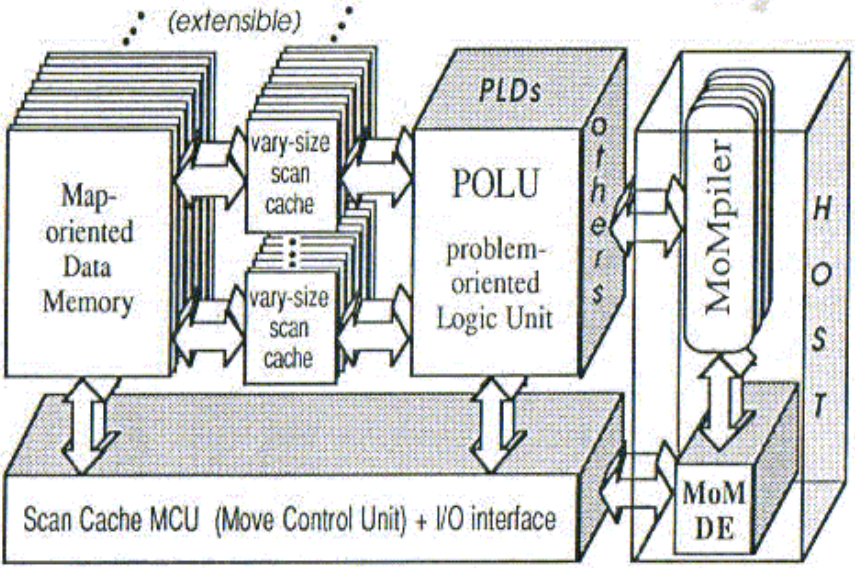
For some algorithms such as e.g. image processing algorithms, a classical software solution on a von Neumann computer is too slow. On the other side a hardware solution on full custom circuits based on a cellular array concept is expensive and very inflexible.

The Solution

The gap between the totally flexible but slow von Neumann solution and the very fast but expensive and inflexible array and pipeline architectures is filled with a medium speed, low cost solution called Map Oriented Machine (MOM). The basic idea of speeding up the algorithms is to parallelize the program access by combinational hardware. Unlike other solutions which pump the data through fixed processor arrays, we use fixed data in a map-organized memory and move special vary-size scan caches across it. This is performed by a universal data sequencer, the Move Control Unit (see figure), which has a simple but powerful instruction set to allow movement across the image in arbitrary directions. A repertory of systematic movements like video scan, spiralic scan, shuffle/butterfly patterns, etc. is

supported and also data-dependent automatic moves such as e.g. contour following are possible.

The contents of the scan cache is matched in parallel with the reference patterns stored in the PLDs (programmable logic devices, or other devices) of the POLU. A match of the actual cache contents with one (or more) of the reference patterns will result in a data manipulation on the map oriented memory.



MOM - Architecture: The figure shows the main parts of the MOM. On the left side the hardware components including the memory, scan cache, POLU and the MCU are shown. The POLU consists of programmable logic devices (PLD) or other devices such as (E)PROMs, RAMs . It is the only programmable part of the hardware, whereas the other parts build the universal part.The MOM Development Environment and the MoMpiler are the software components of the system which run on a host computer.

Results

With our flexible hardware architecture the acceleration factors of specialized hardware solutions cannot be achieved, but this factor is still between 100 and 10000 compared to conventional software programs. A substantial benefit, however, is obtained in the flexibility of the system. MOM is a compromise between special hardware and computer use, not losing the advantages of control side parallelism, but achieving more generality and flexibility.

Image processing is one of the most important application areas of the MOM. To show efficient pattern matching a demo example has been implemented (CMOS design rule check), which applies 800 reference patterns to the cache within a single basic machine cycle. As result, the design rule errors are marked within the data memory.

Due to the flexibilityof MOM, especially the flexible move features not only image preprocesses can be performed, but also algorithms for other applications, where the data can be efficiently stored in a two-dimensional memory, may be implemented on the MOM. Such algorithms are e.g. design rule check, Lee routing, arithmetic problems, matrix operations, systolic algorithms and many others.