Reconfigurable Supercomputing: Hurdles and Chances

(invited presentation)
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Abstract. Reconfigurable Computing (RC) went mainstream in embedded systems already years ago. Astonishingly high hit rates by Google illustrate the pervasiveness of FPGA and RC applications (see http://fpl.org/click/). More recently RC slowly obtains some acceptance within many areas of supercomputing. Cray and Silicon Graphics have launched products including FPGAs used as accelerators. Some application areas report speedup factors by up to two orders of magnitude (and sometimes even more, up to a factor of 6000 so far), as well as the reduction of floor space requirements and of the electricity invoice amount by about one order of magnitude. More is to be expected for the near future. The desktop personal supercomputer is near.

This is astonishing, since the clock frequency of FPGAs is drastically lower than the speed of microprocessors, and, the effective integration density falls behind Moore's law by more than 4 orders of magnitude (The Reconfigurable Computing Paradox). Here algorithmic cleverness is the secret of success on the way to new frontiers in supercomputing. This is based on software to configware migration mechanisms, striving away from memory-cycle-hungry instruction-stream-based computing paradigms (the von Neumann syndrome). Main hurdles on the way to incredible new horizons of cheap highest performance are educational deficits causing the configware / software chasm. Experts with a typical CS background often need the support by EE type colleagues, coming along with communication problems. The talk gives a survey on fundamental issues in reconfigurable supercomputing and on new directions in CS-related curricula.