Bio of Reiner Hartenstein

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Reiner Hartenstein is professor at TU Kaiserslautern and was visiting professor at UC Berkeley. All his degrees are from Karlsruhe Institute of Technology. He is consultant and authorized expert on EDA tools as well as Reconfigurable and Parallel Computing and is credited to be the father of High Performance Reconfigurable Computing (HPRC) and „structured VLSI design“.

He is the creator of the calculus property hardware language KARL, backbone of the world’s first VLSI CAD framework (EU grant: 85 mio ECU), trailblazer for VHDL and Verilog. He also is the founder of the Multi University VLSI Design Project „E.I.S.“ (EU grant: 38 mio DM), the German contribution to the Mead-&-Conway VLSI design revolution and the forerunner of the EUROCHIP action of the EU, still active worldwide. He is founder or co-founder of several successful international annual conference series.

He is IEEE fellow, SDPS fellow, FPL fellow, and recipient of several other awards. He has published 14 books and more than 400 technical papers. More than 100 of his numerous talks are invited presentations, including almost 40 keynote addresses.