

# Early EDA Innovations in Europe driven by Lynn Conway's Lambda Notation

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**Abstract.** This paper summarizes the history of introducing the Mead-&Conway VLSI design revolution in Europe. Although the academic scene in Europe was watching the DARPA-supported break-through in the U.S., all national governments declined support by pointing toward the missing funding in all neighbor countries – a classical deadlock. This paper reports how later the E.I.S. project completely removed this Europe-wide deadlock by stimulating national multi-university programs and spearheading the EURCHIP action still running to-day, supported by the EU commission. The paper details the impact of these programs on various areas in structured VLSI design and computer structures.

Working at Karlsruhe on hardware description languages [1] and microprogramming [2], and teaching digital system design and computer architecture (from 1969 to 1977) I was highly impressed by the colleagues from semiconductor technology with their expensive equipment. I did not expect, that I ever would design the layout of a microchip. Popularized by Bob Rosin's article microprogramming looked interesting at first glance [3]. But I became more and more sceptic: it's also a method to keep the masses of CS people away from the technology scene. Exponentiating the von Neumann syndrome [4] based on nesting several von Neumann machines turned out not to be a desirable VLSI system perspective, so that the German computer society dissolved its special interest group on microprogramming. Going 1977 to Kaiserslautern I started a chair on EDA and computer structures.

Meeting Carver Mead (Professor at Caltech) and Lynn Conway (head, VLSI Lab at Xerox PARC) during a trip to the Design Automation Conference at San Diego in 1979 I learned fascinating details about their VLSI design methodology efforts and received a copy of Lynn Conway's notes from her visiting professorship at MIT and prepublication color copies of the first 4 chapters of their book [6]. Back home to Kaiserslautern I started in summer semester 1979 the first regularly scheduled Mead & Conway style university course with exercises: the first one "on the entire continent" (Asia and Europe except UK). My students became tremendously excited and seized the opportunity of learning by doing. My article about this rapidly spread the news of disruptive developments from the U.S. [7, 8]. I went on to lobby for innovative curricula and prototyping infrastructures as known from MPC79 or MOSIS.

At the annual "Schlosstag" reception at Schloss Birlinghoven on October 1 in 1981 Prof. Dr. Norbert Szypersky celebrated his debut as the new CEO of the GMD. In front of the buffet he had a long talk with me and the queue of guests waiting for shake hands with the new CEO was growing longer and longer. Just back home as visiting professor at UC Berkeley I was a legendary animal to him, since he just started founding the „International Computer Science Institute (ICSI)“ at Berkeley. VLSI became a very important matter of the boss and Dr. Woelcken, head of Prof. Szypersky's staff, was put into charge at very high priority.

Soon a 3 day tutorial (more than 30 professors „back to the school bench“) has been organized with me as the only speaker coming with boxes full of transparencies (PowerPoint did not yet exist). Because of the strong demand a second run has been organized a few weeks later. During the evening social activities a pressure group has been formed, since „the industry“ combatted us. „Lobbyism prevents a balanced industry policy and efficient research funding“ [9]. Such a pressure group has been urgently needed, also throughout Europe (except UK and Scandinavia), where for years the professors Carlos Lopez-Barrio (Spain), Francois Anceau (France), Heetmann (The Netherlands), Roger Van Overstraeten and Hugo De Man (Belgium), Mariagiovanna Sami and Luigi Dadda (Italy), etc. could not convince their governments. This formed a classical deadlock by the argument, that all neighbor countries do not do anything. Let me illustrate our hostile environment. My first proposal to the BMFT (Ministry of Research and Technology) failed because of the industry lobby and the favorite reviewer of the responsible department, a semiconductor technology professor, who characterized Carver Mead as a charlatan. He claimed, that, instead of going to Coyote Hill Drive (where MPC79 had been organized) he went to Deer Creek Road (the fabrication site) to find out the real truth. For me this first attempt ended with an embarrassing first class throw out.

The Europe-wide deadlock finally has been broken by Germany via my successful second proposal. Promising a political change Helmut Kohl became Bundeskanzler in 1983. But for me the turning point has been the new Technology Minister Dr. Heinz Riesenhuber, almost a kind of old friend of mine. Another turning point has been, that another person became the head of his responsible BMFT department who finally signed a document providing for us a grant of 35 million Deutschmark for 3 years to run the German multi university project. Didn't he know, that he should have asked for permission by „the industry“? Or, did he sign

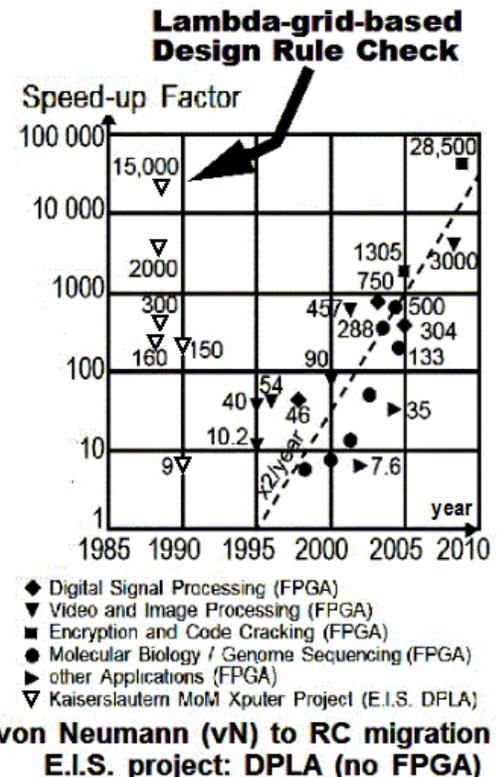


Figure 1. Speed-up factors obtained by von Neumann to Reconfigurable Computing (vN to RC) migration.

with a wink ? In 1987 this „E.I.S. Projekt“ [10-12] has been extended by another 18 months with a second grant (E.I.S. stands for „Entwurf Integrierter Schaltungen“).

The “E.I.S. Projekt” headed by me and massively supported by Dr. Klaus Woelcken from GMD was very productive, and became the incubator of the EUROCHIP service, also, since in 1988 Dr. Woelcken became an officer of the Commission of the European Union. In 1988, the CEC launched a call for tenders to select a consortium to serve European universities for several services including multi project chip fabrication. As a result, the EUROCHIP organization was set up including CMP from France, the German E.I.S project, the Inter-University Center for Microelectronics (IMEC) in Belgium, NORCHIP from Scandinavia, and the Rutherford Appleton Laboratory (RAL) in the UK. Finally 417 academic institutions participated, training about 15,000 students per year; about 16,000 copies of 20 different CAD packages were distributed and about 200 multi project wafer batches have been fabricated, containing some 2700 circuits [11]. EUROCHIP also supported activities in Latin America (IBERCHIP) and Eastern Europe (EUROEAST). Of course, bootstrapping the learning process in these countries has the positive side-effect of encouraging the development of potential future markets for European industry. In 1995 EUROCHIP launched EUROPRACTICE, designed to cover a broad range of systems orientated technologies and its services targeted to academia and to all types of industrial users by including training, design packages and access to prototype manufacturing and packaging.

During my stay as a visiting professor at UC Berkeley in 1981 I could learn lot, like experiencing ARPANET access to the MOSIS service housed in Marina del Rey. I collected valuable experience in using many tools providing direct support for „Mead-&-Conway design“, like a design rule checker, a circuit extractor, the MOSSII switch-level simulator, a silicon compiler, and the IC layout tools CAESAR and MAGIC. The availability of all these Mead-&-Conway-based tools made UC Berkeley an incubator of the later EDA software industry, including Cadence, Mentor Graphics, Viewlogic and many others. Carlo Sequin, also my sponsor at UCB, consulted Lynn Conway and took me with him for a ride to PARC at several Wednesdays. Having me as a medium UCB and PARC also was at least partially an incubator of the E.I.S., CVT and CVS projects.

Circuit extraction became mandatory for most IC design processes. EDA tools to generate and check layouts were massively simplified and speeded-up by Lambda-based methods. With this scalable design rule methodology we at Kaiserslautern implemented in the early 80ies a design rule check called PISA [13, 14] on our MoM architecture [15] by adapting image preprocessing methods for interpreting a Lambda-grid based circuit design file as a pixel array. A 4-by-4 pixel scan window scanned this array pixel by pixel and line by line (a video scan). For each scan window position the 4-by-4 pixel design pattern is compared in parallel with several hundred rule violation reference patterns. Because of this parallelism only a single clock cycle is needed for each scan window position.

Since first FPGAs appearing on the market in 1984 have been tiny, we designed our own PLA-like chip called „DPLA“ (Dynamically Programmable Logic Array), manufactured via E.I.S. project Multi Project Chip organization. This extremely area-efficient solution was possible by using sum of product Boolean expressions for all reference patterns, so that a we did not need the less area-efficient FPGAs. Compared to a software-only version on a Motorola 68020 we obtained a speed-up factor of more than 15.000 (fifteen-thousand) – 20 years before similar factors have been reported from the FPGA scene (see Fig. 2). This massively outstanding competitive edge in vN to RC migration would have been impossible without Lynn Conway’s scalable design rule methodology. During my time at UC Berkeley I learnt PLA design and the M-&-C EDA infrastructures created and organized by Carlo Sequin and his people. PISA is also an early application of our Anti Machine paradigm (counterpart of the von Neumann machine by using data counters instead of a program counter [15, 16]). Based on this methodology we also implemented multi-level extractor supporting automatic test pattern generation efforts [17, 18].

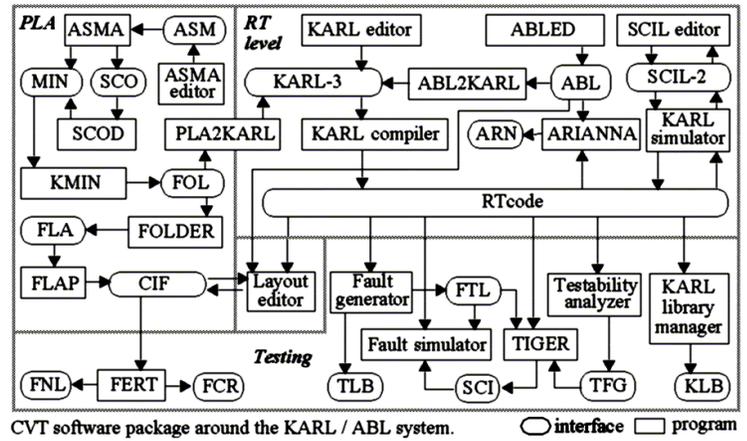


Figure 2: The worldwide first VLSI CAD framework: for the acronyms and for their meanings see figure 3.

#### Acronyms from the CVT / CVT CAD framework

<b>ABL</b>	<b>A Blockdiagram Language (KARL graphic sister language)</b>
<b>ABLED</b>	<b>ABL EDitor</b>
<b>ABAKUS</b>	<b>ABL And KARL USer Group</b>
<b>ARIANNA</b>	<b>Interactive chip floor plan generator</b>
<b>ASMA</b>	<b>Algorithmic State Machine Assembler</b>
<b>BACH</b>	<b>Behavioral-Level Automated Compilation of Hardware</b>
<b>CVS_BK</b>	<b>CVS Behavioral KARL (KARL with nested machines extension)</b>
<b>FELIX</b>	<b>Design space exploration Framework (KARL calculus inspired)</b>
<b>FERT</b>	<b>Fault model Extractor at RT level</b>
<b>FLAP</b>	<b>MOS layout generator for PLAs, MOL and other logic</b>
<b>FOLD</b>	<b>PLA FOLDing tool</b>
<b>hyperKARL</b>	<b>KARL filter front end for generic and recursive descriptions</b>
<b>KARATE</b>	<b>KARL Automatic Test Extractor</b>
<b>KAPA</b>	<b>KARL dialect (Porto Allegre)</b>
<b>KARL</b>	<b>KArlsruhe (KAiserslautern) stRuctured design calculus Language</b>
<b>KMIN</b>	<b>Logic Minimization tool</b>
<b>OFGKA</b>	<b>Olivetti Fault Generator for nets described in KARL</b>
<b>OFSKA</b>	<b>Olivetti Fault Simulator based on KARL</b>
<b>OTAKA</b>	<b>Olivetti Testability Analyser based on KARL</b>
<b>PSICO</b>	<b>a System for Automatic Layout Synthesis</b>
<b>REX</b>	<b>Extracting KARL descriptions from layout</b>
<b>SCIL</b>	<b>Simulator Control and I/O Language</b>
<b>SCOD</b>	<b>State Encoding tool</b>
<b>SMART</b>	<b>SiMulator At Register Transfer level</b>
<b>superKARL</b>	<b>KARL filter front end to extract PLAs and other logic</b>
<b>SYS3</b>	<b>Systolic Array Syntesis System</b>
<b>TIGER</b>	<b>Test pattern Interactive Generator Environment at RT level</b>
<b>VERENA</b>	<b>Automatic verification of KARL descriptions</b>

Figure 3: CVS Acronyms, mostly also used within Fig. 2.

Immediately after my talks on KARL during a summer school at Scuola Reiss-Romoli (L'Aquila, Italy), I have been asked to join the CVT proposal („CAD for VLSI in Telecommunications“), headed by Dr. Leproni at CSELT at Torino, Italy. CSELT SPA has been the STET Group's Company for study, research, experimentation and qualification in Telecommunications and Information Technology [19]. CSELT, sometimes called „The Italian Bell Labs“, founded 1964, about 1200 employees, has been a highly respected think tank [19]. Later the name changed into Telecom Italia Lab, when some investors filleted it, so that the famous CSELT culture disappeared.

The CVT proposal and its successor CVS („CAD for VLSI Systems“) have been funded by the CEC with about 85 million € (at that time called „ECU“). The final result has been a fully fledged VLSI design framework including an interactive and automatic fault model and test pattern generation and analysis, a state machine encoder and assembler, an automatic floorplan generator, automatic systolic array, MOL and PLA generation, minimization and folding, as well as automatic verification of KARL descriptions (figure 2 and 3). CVT and CVS massively demonstrated that Lynn Conway's scalable design rules have dramatic implications for all facets of tool-building and chip prototyping by the worldwide first complete VLSI CAD framework, years before this term has been coined elsewhere.

CVT and CVS also provided a major break-through for the KARL and ABL design calculus language methodology [20] and extensive support [21] to its user community [22]. ABL followed Lynn Conway's recommendations by our Domino notation where adjacent cells or subsystems could be abutted by structured design of their cells at systematic pitch ratios. This Domino notation is the basis of ABL as KARL's floorplan language and graphic interface. Used worldwide during the 80ies KARL has been a trailblazer of VHDL. As soon as the first preliminary paper appeared about VHDL the EU commission stopped funding, not only CVS/CVT with KARL, but EDA research in general [23]. But not supporting layout, floor planning and other Mead-&-Conway aspects, VHDL was a much worse choice: "... Adoption of VHDL was one of the biggest mistakes in the history of design automation, causing users and EDA vendors to waste hundreds of millions of dollars..." said Joe Costello in 1995 when being CEO of Cadence Design Systems [24]. Currently the dominance of VHDL – difficult to use - is a major hurdle in finding a way out of the dramatic MPSoC programming crisis by going toward an inevitable heterogeneous methodology of system design and programming [5, 25 - 27]. Later KARL versions with procedural extensions have supported twin-paradigm methods for such heterogeneous system synthesis [28].

<b>Industry Partners:</b>	INRIA
AEG-Telefunken	Italtel
Alcatel	MATRA-MHS
British Telecom*	Olivetti
CENG LETI	SGS
CNET	Standard Elektrik Lorenz
CSELT	ST Microelectronics
Daimler Benz	THOMSON EFCIS
DBP Research Inst.	<b>Universities:</b> Aachen,
DECNET	Bologna, Bremen,
GMD	Darmstadt, Dortmund,
HONEYWELL BULL	Genova, Kaiserslautern
IMAG	Karlsruhe, Milano, Torino

**Figure 4: CVT and CVS partners.**

## About the Author

Reiner Hartenstein is full professor of the Technical University of Kaiserslautern, where he founded a chair on EDA and computer structures. He received his diploma degree (in 1959) and his Dr.-Ing. degree from the Karlsruhe Institute of Technology (KIT) as a scholar of Prof. Karl Steinbuch, a very early pioneer of artificial neural networks. Reiner has been a researcher in image processing and computer structures. From 1969 until 1977 he was associate professor at KIT. In 1981 he has been visiting professor at University of California in Berkeley. He is IEEE fellow, SDPS fellow, FPL fellow and received several best paper awards. Reiner is founder and/or co-founder of several international annual conference series still running successfully. He has been sometimes general chair and more often program chair of international conferences. As a well-known evangelist of High Performance Reconfigurable Computing Reiner's hobby is opening international conferences by a keynote address. For instance with his 37<sup>th</sup> keynote he opened the ISCAS 2011 at Rio de Janeiro with about 900 attendees.

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