Reiner Hartenstein, eingeladener Beitrag (invited presentation)

Programmierung Rekonfigurierbarer Schaltungen:

nur Logik-Synthese auf einer seltsamen Nischen-Plattform?

Reiner Hartenstein

Terminology & Acronyms

- RC: reconfigurable computing
- RL: reconfigurable logic
- Software (SW): procedural sources
- Configware (CW): structural sources
- Hardware (HW): hardwired platforms
- ASIC: customizable hardwired platforms
- Flexware (FW): reconfigurable platforms
- FPGA: field-programmable gate array
- FPL: field-programmable logic

*note: firmware is SW!

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Perspektiven

- (b. u. Verziehung für englischsprachige Folien)
- schwierig aus der Frosch-Perspektive
- bekannte HW/SW-Kommunikations-Barrieren
- Orientierung durch die Vogel-Perspektive:
  - Verstehen des Paradigmen-Wechsels
  - Spürsinn und Verständnis für die Trends

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Overview

- The New Paradigm
- Coarse Grain
- Data Sequencing
  - cope with the 2nd Design Crisis
- Conclusions

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Heraus aus der Nische

- bisher: Logik-Entwurf, i. e. "Hardware"-Entwurf für eine seltsame Plattform
  - CAD statt Compilation
- jetzt sichtbar: System-Denken, Lehrgebäude
- kommende Dichotomie der Informatik
  - SW <-> CW
  - HW <-> FW
  - computing in time <-> computing in space

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The New Paradigm

- The New Paradigm
  - going Mainstream
- Data Sequencing
  - cope with the 2nd Design Crisis
- Conclusions

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Changing Models of Computing

- Software: Configurable (structural)
- Downloading
- RAM
- I/O
- Instruction sequencer
- Contemporary computing
- Hardwired computing
- Flexware

Sequential vs. structural RAM

- Logic Synthesis
- Route and Place
- FPGA
- Structural RAM
- Download

Basics of Binding Time

- Time of "Instruction Fetch"
- Run time
- Loading time
- Compile time
- Reconfigurable Computing

Dataquest Predicts Programmability will be Predominant in SOC

- Application-specific programmable products (ASPPs) will be the next best thing in semiconductor technology
- With programmability as a standard feature, ASPPs will be predominant system-on-a-chip products in five years

Makimoto’s Wave

- Nick Makimoto
- Designer of the Motorola 88000
- "The Programmable System-on-a-chip is the next wave in the chip industry’s historic shifting between custom and standard parts."

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History of Silicon Application

Stone Age
(Rubyliith, ...)
(CAD, netlist)

Bronze Age
(Compilers...)
(FPGAs: CAD...)
machine paradigm

Configware Age
no further shift?
no 3rd wave?
resources variable
coarse-grain dynamically reconfigurable

Makimoto’s 3rd Wave
earlier than 2007
coarse grain dynamically reconfigurable
(highly efficient, if domain-specific)

universal FPGA?

FPGA Performance vs. KressArray

FPGA Performance

Stone Age
using Design Method for Hardwired ...
(Live Synthesis mainly)

Makimoto’s 3rd Wave

• FPGAs:
  - 1st half of 3rd wave
    - universal (but less efficient):
  - Coarse Grain Subsystems:
    - 2nd half of 3rd wave
      - domain-specific
      - much more flexible than 2nd half of 2nd wave

Applications

• next generations’ wireless*
• network processors*
• many other areas*

*) keynotes and papers at FPL 2000
Villach, Austria, August 27 - 30, 2000
http://www.fpl.uni-kl.de/FPL/

The 10th International Conference on Field-programmable Logic and Applications
The Roadmap to Reconfigurable Systems
Coarse Grain reconfigurable

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Conformable Computing Systems

• combine programmable sequential processor with structurally programmable "hardware"
• capitalize on the strength of both, hardware and software.
• early 60s: Estrin (UCLA): enabling technology not available
• 90s: significant increase of research activities (DARPA ...)
• FPGAs: not the enabling technology; hardware skills needed
• Verilog or VHDL based systems often result in poor performance

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PE Architecture of KressArray

Area-efficient
Multiple user-based
Routing Resources
inside PE cell
No Routing Channels
array scalable

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Examples

Domain-specific KressArrays

array mapper supports:
segmentation
predefined macros
manual modification
port location constraints

more than 2 buses...

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KressArray-1: Mapping Example

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KressArrayFamily

Communication Architecture by Examples

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Kresse Array Design Space Xplorer

Platform available

- Soft Data Path Arrays (experimental):
  - Matrix (M.I.T.)
  - Kresse Array
  - CHESS Array (Hewlett Packard)
  - many others
- Compilation techniques feasibility studies:
  - Partitioning Co-Compiler
  - Design Space Explorer
  - others

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Xplorer Mapping of SNN filter

Platforms available

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von Neumann is obsolete

Multiple sequencers make sense

like a Systolic Array
array of PUs (processing units)

High Memory Bandwidth

Sequencers by Reconfiguration

Generic Address Sequences
MoPL Language Features

- Atomic Scan Pattern defined by
  - Step Vector
  - min. Length
- Compound Scan Pattern defined by
  - Chains,
  - Looping Chains,
  - Nesting,
  - Parallelism

Any Scan Pattern may be adapted at Run Time:
- Premature Termination at Run Time** by "Escape"
  - base or limit threshold
  - decision data
  - decision data short cut
  - event
  - data tag
  - tagged control word

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Scan Pattern Editor

- ready for Soft Machine Paradigm
  - DD-driven* (instead of control-flow-driven)
  - i.e. data-procedural (not control-procedural)
  - deterministic (no "data flow machine")
  - supporting soft data paths
  - supporting data path arrays (i.e. KressArray)
  - supporting multiple I/O data streams

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Fundamental Ideas available

- Data Sequencer Methodology
- Data-procedural Languages (Duality w. v. N.)
- ... supporting memory bandwidth optimization
- Soft Data Path Synthesis Algorithms
- Parallelizing Loop Transformation Methods
- Compilers supporting Soft Machines
- SW / CW Partitioning Co-Compilers

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cope with the 2nd Design Crisis

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From Synthesis to Compilation

Logic Synthesis
Download
Structural Compiler

High Level Language Source
Download

FPGA
Coarse Grain
Machine Paradigm

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Conclusions

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Makimoto's Law revisited

- The accelerated information economy lives from rapid technology progress
- A slow down of the Gordon Moore curve will cause a severe economy crisis
- A remedy: narrowing the design gap: not possible just by better architectures
- When Gordon Moore’s Curve slows down only RC usage can keep innovation speed

The END
GAG and Stepper

Applications (1)

new cellular standard: up to 2 Mb/s/sec;
new CDMA standard: > 500 MIPS needed just for RF receiver part

wide variety of end-user’s devices:
smart phones, palm pilots, laptops, games, camcorder-like, ...
the internet car, many new types of devices to come ...

increasing wide variety of services available from network provider:
download just what a particular customer is subscribed to export group [Visser]: > 2% of it will be accelerator code*

Applications (2)

Image Processing:
for smart cars (collision avoidance, others ...),
smart traffic pilots, robotics, fast material inspection,
smart stub finders, motion detection (MPEG-1). ...

Signal Processing, Speech Processing, Software Radio,
Correlation, Encryption, Comm Switching / Protocols,
Innovative-consumer electronics:
super smart cards, smart handles, wearable,
portable, set-top, laptop, desktop, embedded, ...
many others, ...

Applications (3)

JPEG zigzag scan pattern

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CGFFT: Nested and Parallel Scan Pattern

KressArray Reconfigurability

Overview of the MDS

"Programming" Domains

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"Programming" Domains

<table>
<thead>
<tr>
<th>Platform</th>
<th>Personalization (&quot;Programs&quot;) by</th>
<th>Programming Domain</th>
<th>Communication Paths Setup Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware</td>
<td>CAD</td>
<td>Space</td>
<td>Fabrication/Time</td>
</tr>
<tr>
<td>Systolic Array</td>
<td>CAD</td>
<td>Time and Space</td>
<td>Fabrication/Time</td>
</tr>
<tr>
<td>procedural (e.g., &quot;von Neumann&quot;)</td>
<td>Software</td>
<td>Time</td>
<td>Run Time</td>
</tr>
<tr>
<td>Flowchart</td>
<td>Configure</td>
<td>Space</td>
<td>Compile Time</td>
</tr>
<tr>
<td>Embedded Flowchart</td>
<td>Configure / Software Co-Compilation</td>
<td>Time and Space</td>
<td>Compile and Run Time</td>
</tr>
</tbody>
</table>

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Applications

new cellular standard: up to 2 Mbit/sec: new CDMA standard: > 500 MIPS needed just for RF receiver part
wide variety of end-user’s devices: smart handles, palm pilots, laptops, games, camcorder-likes, ...the internet car, many new types of devices to come ...
increasing wide variety of services available from network provider: download just what a particular customer is subscribed to
expert group [Visser]: > 20% of it will be accelerator code*

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Applications (2)

Image Processing:
- for smart car (collision avoidance, others ...),
- smart traffic pilots, robotics, fast material inspection,
- smart stub finders, motion detection (MPEG-4, ...)
Signal Processing, Speech Processing, Software Radio,
Correlation, Encryption, Comm. Switching / Protocols,
Innovative consumer electronics:
- super smart cards, smart handles, wearable,
- portable, set-top, laptop, desktop, embedded, ...
- many others, ...

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Also as an Autonomous Machine

New Machine Paradigm (Xputer)
is the counterpart of the so-called von Neumann paradigm
- CONS: confuses customers (paradigm switch: the brain hurts)
- PROS: strong guidance of EDA tool development
- more effective hardware/software APIs
- compilation techniques similar to traditional compilation
- better Application Development Tools accepting C or Java
easy to teach: simple machine principles
- scan patterns (data counter) similar to control flow (program counter)
- general model of hardware / software co-design
- fascination for freak effect: opening up a new R&D discipline

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The Microprocessor is a Methuselah

- 1st: 4004
- 2nd: 8008
- 3rd: 8086
- 4th: 80286
- 5th: 80386
- 6th: 80486
- 7th: P5 (Pentium)
- 8th: P6 (Pentium Pro / Pentium II)
- 9th: Pentium III

9 technology generations ... the steam engine of the silicon age

In Contemporary Desktop and Embedded Systems Most of the Silicon Real Estate is Occupied by Accelerators - A Symptom of the Limitations of the Microprocessor

WWW goes Wireless

- Palm VII
- Winworld
- WWW goes Wireless

Scan pattern entry
task composer generate report

Task Designer

- the Task Designer is a graphical programming tool for the data sequencer

Application Chooser

- design flow illustrated
- each design step represents active
- only possible actions at a specific design step activated

Task Composer

- the task composing step allows to construct complex scans out of several scan pattern

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Reiner Hartenstein, eingeladener Beitrag (invited presentation)

Scan Pattern Editor

Reconfigurable Computing Developments -- Trends
Reiner W. Hartenstein
Universität Kaiserslautern

EH / ES (Conferences): Evolvable...

NASA/DoD Workshop on Evolvable Hardware
Sponsoring:
National Aeronautics and Space Administration (NASA)
Defense Advanced Research Projects Agency (DARPA)
Ballistic Missile Defense Organization (BMDO)

EH'99: Impact of Evolvable Hardware
- The emerging field of Evolvable Hardware is expected to have major impact on deployable systems for space missions and defense applications that need to survive and perform at optimal functionality during long duration in unknown, harsh and/or changing environments.
- Examples of such applications include outer solar system exploration, missions to comets and planets with severe environmental conditions, long lasting space-based surveillance platforms, defence countermeasures, long-term nuclear waste and other hazardous environment monitoring and control.
- Evolvable hardware is also expected to greatly enrich the area of commercial applications in which adaptive information processing is needed; such applications range from human-oriented hardware interfaces and Internet adaptive hardware to automotive applications.

Evolvable Hardware Evolution Cycle

Classification of Configware

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• (same building)
• Herrn Wasenmüller fragen

SPARE:

FPGA Performance vs. KressArray

e. g. KressArray:
- 18 bit PU cell
- 8 NNports
- 4 boxes
- 0.18 µm CMOS:
- 0.06 mm² area

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